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Nitric acid oxidation of Si (NAOS) method for low temperature fabrication of SiO_2/Si and SiO_2/SiC structures

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ABSTRACT

We have developed low temperature formation methods of SiO_2/Si and SiO_2/SiC structures by use of nitric acid, i.e., nitric acid oxidation of Si (or SiC) (NAOS) methods. By use of the azeotropic NAOS method (i.e., immersion in 68 wt% HNO_3 aqueous solutions at 120 °C), an ultrathin (i.e., 1.3–1.4 nm) SiO_2 layer with a low leakage current density can be formed on Si. The leakage current density can be further decreased by post-metallization anneal (PMA) at 200 °C in hydrogen atmosphere, and consequently the leakage current density at the gate bias voltage of 1 V becomes 1/4–1/20 of that of an ultrathin (i.e., 1.5 nm) thermal oxide layer usually formed at temperatures between 800 and 900 °C. The low leakage current density is attributable to (i) low interface state density, (ii) low SiO_2 gap-state density, and (iii) high band discontinuity energy at the SiO_2/Si interface arising from the high atomic density of the NAOS SiO_2 layer.

For the formation of a relatively thick (i.e., ≥10 nm) SiO_2 layer, we have developed the two-step NAOS method in which the initial and subsequent oxidation is performed by immersion in ~40 wt% HNO_3 and azeotropic HNO_3 aqueous solutions, respectively. In this case, the SiO_2 formation rate does not depend on the Si surface orientation. Using the two-step NAOS method, a uniform thickness SiO_2 layer can be formed even on the rough surface of poly-crystalline Si thin films. The atomic density of the two-step NAOS SiO_2 layer is slightly higher than that for thermal oxide. When PMA at 250 °C in hydrogen is performed on the two-step NAOS SiO_2 layer, the current–voltage and capacitance–voltage characteristics become as good as those for thermal oxide formed at 900 °C.

A relatively thick (i.e., ≥10 nm) SiO_2 layer can also be formed on SiC at 120 °C by use of the two-step NAOS method. With no treatment before the NAOS method, the leakage current density is very high, but by heat treatment at 400 °C in pure hydrogen, the leakage current density is decreased by approximately seven orders of magnitude. The hydrogen treatment greatly smoothens the SiC surface, and the subsequent NAOS method results in the formation of an atomically smooth SiO_2/SiC interface and a uniform thickness SiO_2.

1. Introduction

Silicon dioxide (SiO_2)/Si system is a fundamental structure for large scale integration (LSI) and thin film transistors (TFT). In the case of LSI, a gate oxide layer is usually formed by thermal oxidation of Si above 800 °C. Thermal oxidation is generally considered to be the best method for the formation of SiO_2/Si structure. However, a serious problem arises in the case of ultrathin SiO_2/Si structure, i.e., high leakage current density. In fact, the leakage current density flowing through SiO_2 exceeds the gate limit of 1 A/cm^2 (e.g., at the gate bias of 1 V) when the SiO_2 thickness is below 1.5 nm [1–3], and thus the device operation becomes impossible. Interfacial stress cannot be avoided because of the difference between the thermal oxidation and device operation temperatures. Another disadvantage of thermal oxidation is that the oxidation rate strongly depends on Si surface orientations [4], which makes it difficult to form a uniform thickness SiO_2 layer, e.g., on trench structure and poly-crystalline Si (poly-Si) surfaces.

Thin film transistors (TFT) for operation of liquid crystal display, organic electroluminescence (EL) display, etc., are currently produced on glass substrates. Therefore, a gate insulating layer should be produced at temperatures below ~450 °C. The conventional method to form a gate oxide layer at low temperatures utilizes deposition such as plasma-enhanced chemical vapor deposition (PECVD) [5–7]. However, the interfacial properties of the deposited SiO_2 films are much worse than those produced by direct oxidation methods such as thermal oxidation because initial surfaces before deposition become SiO_2/Si interfaces after deposition, and thus surface contamination and incomplete bond formation at the interface cannot be avoided. Moreover, using the deposition

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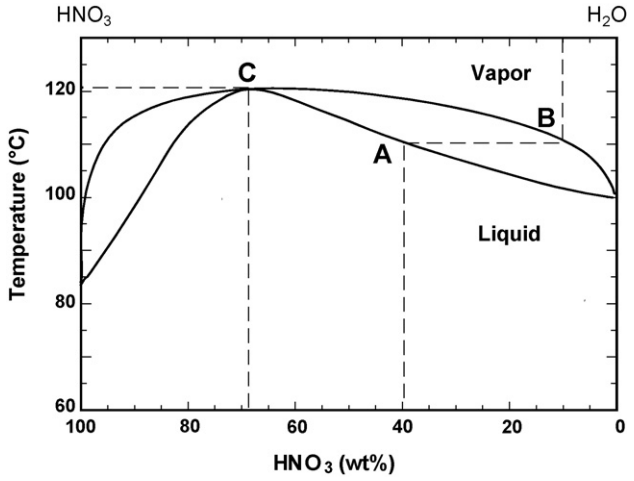

Fig. 1. Phase diagram of HNO_3/H_2O system.

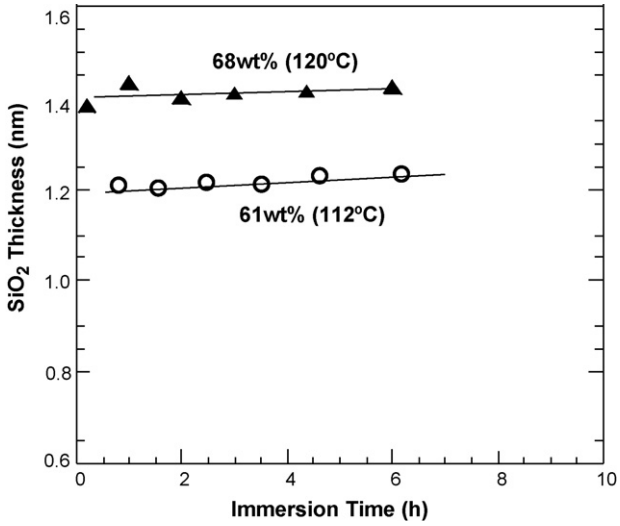

Fig. 2. Thickness of the SiO_2 layer formed by immersion of Si in 61 and 68 wt% HNO_3 solutions vs. the immersion time.

method, uniform thickness SiO_2 layer cannot be formed especially on rough poly-Si surfaces (i.e., ridge structure) which results from laser annealing of amorphous Si thin films to crystallize [8]. To prevent a high density leakage current flowing through thin top regions in the ridge structure, a relatively thick gate oxide layer in the range between 50 and 100 nm should be formed. The thick gate oxide layer makes it difficult to miniaturize TFT. In fact, submicron size TFT in practical use has not been realized so far. Moreover, an operation voltage of TFT largely increases with the thickness of the gate oxide layer, and power consumption is proportional to the square of the operation voltage. Therefore, shrinkage of the gate oxide thickness leads to a vast decrease in the TFT power consumption. The bulk properties of deposited SiO_2 films are also poor, due to inclusion of carbon species, OH species [9], etc., and to less-dense structure.

The above problems can be avoided by direct oxidation methods at low temperatures. Several low temperature direct Si oxidation methods have been developed, e.g., plasma oxidation [10,11], photo-enhanced oxidation [12], metal-promoted oxidation [13,14], ozone oxidation [15,16], etc. We have also developed a low temperature direct oxidation method called nitric acid oxidation of Si (NAOS) method which utilizes strong oxidizing activity of azeotropic mixture of nitric acid (HNO_3) and water (i.e., 68 wt% HNO_3 aqueous solutions) [17–22]. In the present paper, we have reviewed the studies on the NAOS methods to produce (i) ultrathin SiO_2/Si structure with a low leakage current density [17–20], (ii) relatively thick (i.e., 10–30 nm) SiO_2/Si structure with good electrical characteristics [21–23], and (iii) relatively thick SiO_2/SiC structure with an atomically smooth interface [24–26]. All the NAOS methods can be performed at temperatures as low as 120 °C (i.e., below the azeotropic point of 68 wt% HNO_3 aqueous solutions).

2. Azeotropic NAOS method [17–22]

Phosphorus-doped n-type Si(1 0 0) and Si(1 1 1) wafers with ~10 Ω cm resistivity were cleared using the RCA method [27] and etched with dilute hydrofluoric acid (DHF). Then, the Si wafers were immersed in azeotropic mixture of HNO_3 and water (i.e., 68 wt% HNO_3 aqueous solution). Fig. 1 shows the phase diagram of HNO_3 plus water system. It is seen that the boiling temperature of 40 wt% HNO_3 is 108 °C (point A) and the HNO_3 concentration of the gas phase at the boiling temperature is ~10 wt% (point B). Therefore, the concentration of the liquid phase increases with the boiling time due to evaporation of low concentration HNO_3. On the other hand, when 68 wt% HNO_3 is boiling at 120.7 °C (i.e., azeotropic point), the concentrations of the liquid and gas phases are both 68 wt% (point C). Therefore, the concentration of the liquid phase is constant even when boiling is kept at the azeotropic point, and hence stable oxidation can be performed by use of 68 wt% HNO_3 aqueous solutions.

After oxidation with 68 wt% HNO_3, aluminum (Al) electrodes of 0.15 or 0.3 mm diameter were deposited by the thermal evaporation method, resulting in the <Al/SiO_2/Si> MOS structure.

Fig. 2 shows the SiO_2 thickness on the Si(1 0 0) substrate as a function of immersion time in 61 and 68 wt% HNO_3 at their boiling temperatures (i.e., 112 and 120 °C, respectively). The thickness reached 1.2 and 1.4 nm by oxidation with 61 and 68 wt% HNO_3, respectively, within 10 min, and prolonged oxidation did not increase the SiO_2 thickness.

Fig. 3 shows the current–voltage (I–V) curves for the <Al/SiO_2/n-Si(1 0 0)> MOS diodes with the SiO_2 layer formed in 61 (a) and 68 wt% (b) HNO_3 aqueous solutions at their boiling temperatures. The thickness of the SiO_2 layer formed in 61 and 68 wt% HNO_3 was determined to be 1.2 and 1.4 nm, respectively, as described above. The arrow shows the leakage current density for an SiO_2 layer thermally grown usually at temperatures in the range between 800 and

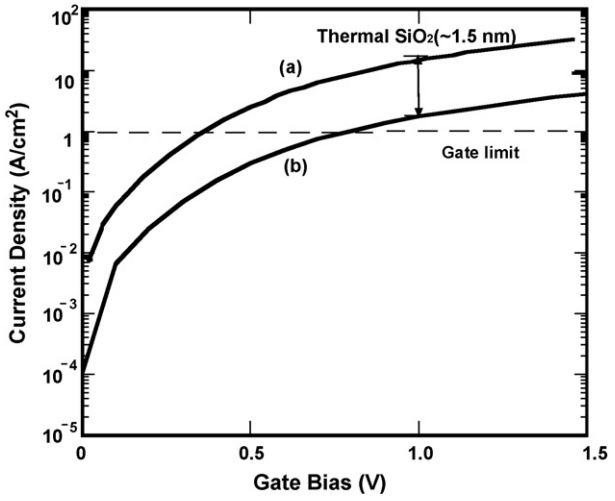

Fig. 3. I–V curves for the <Al/ultrathin SiO_2/Si(1 0 0)> MOS diodes with the SiO_2 layer formed in HNO_3 aqueous solutions with the following concentrations: (a) 61 wt%; (b) 68 wt%.