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Effect of deuterium on passivation of Si surfaces

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ABSTRACT

A properly passivated silicon surface is chemically stable, and all interface properties are constant. The freshly etched Si surface is full of dangling bonds resulting in high surface activity and instability. Hydrogen treatment is a proper procedure to decrease the number of dangling bonds. We demonstrated that deuterium adsorbs on Si surface at room temperature much stronger than hydrogen. Moreover, in case of deuterium-passivated wafers the vacuum storage can be omitted without risking the non-controlled native oxidation of silicon for up to 5 h or more. It could be a suitable and more robust surface cleaning and passivation process for the industry, but heavy water is expensive. As a cheaper procedure, we showed that 1 min vapor phase treatment at 65 °C of heavy water (D_2O) + 50% HF (e.g. 20:1) mixture was enough to remove the native oxide and to passivate the Si surface without any degradation of the atomic surface flatness. The surface evolution of the D-passivated surface was followed by contact angle measurements, spectroscopic ellipsometry (SE), atomic force microscopy (AFM), X-ray photoelectron spectroscopy (XPS), transmission electron microscopy (TEM), infrared absorption spectroscopy (IR), surface potential and surface photovoltage (SPV) mapping and light induced potential transient method. Qualification and the results were compared to the H-passivated, bare and native oxide covered Si surface. Our passivation test results confirmed that using D-passivation on Si surface is a promising method in the MOS technology and the interface engineering processes.

1. Introduction

Semiconductor surfaces are extremely sensitive to the environment, thus the passivation of their surfaces is very important. Some aspects (namely the construction and technology of electron devices and integrated circuits, and the characterisation of the silicon surface and bulk properties) as well as some passivation mechanisms (control of the surface potential barrier and lowering the surface and interface trap densities) have been discussed earlier [1], mainly in conjunction with the bare, oxide covered and porous Si covered [2] silicon surface.

Chemical stability can be achieved by using thermal oxide or other dielectric over-layers. Halogens are used for passivating the bare silicon surface to decrease surface recombination velocity [3]. The properties of the bare and of the oxide covered silicon have been discussed earlier [1]. The silicon covered by an ultra-thin (tunnelable) insulator (native SiO_2) layer has some peculiarities, i.e. connection between surface charge and the interface charge carrier density, which result in depletion or near intrinsic conditions on the silicon surface. Thick insulators usually result in accumulation on n-type, depletion or inversion on p-type silicon, due to positive interface charge on the interface states.

Charging up the insulator surface, the previously discussed surface conditions can be altered, consequently the surface charge may have some passivating effect [4]. This effect has no importance in the device technology, because of its short duration and possible instabilities. However, the ability of surface potential adjustment may help in the characterisation of the silicon surface and bulk properties.

On the other hand, wet cleaning processes, including DHF dip of Si wafers, play a major role in device properties and performance, process yield and reliability, as the electric behavior of the dielectric/silicon interface is strongly influenced by its defect structure. For example, in case of 65 nm node and below, the formation of 1.5 nm thick (or thin) gate oxide/oxy-nitride/dielectric with high reliability is of utmost importance [5]. Nevertheless, further development is needed to improve the performance of the wet chemical cleaning method in order to create ultraclean, smooth and defect-free Si surface with excellent passivation against native oxidation in clean-room atmosphere. Recently, research has focused on hydrogen-terminated passivation of smooth silicon surfaces on the atomic scale due to their cleanliness and excellent electronic properties [6–8].

The first thermal hydrogen desorption peak from a hydrogen-passivated Si surface in vacuum or inert gas ambient can be

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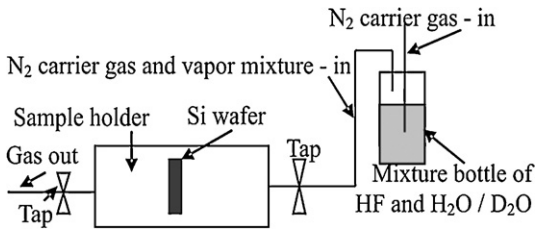

Fig. 1. Schematic draft of the experimental setup for vapor phase treatments. The Si wafer and the whole system were kept at the same temperature (65 °C).

detected at around 380 °C [9]. At around 480–500 °C dangling bonds are generated on the silicon surface by desorption of the remaining hydrogen [10]. At that moment the silicon surface becomes extremely reactive. This phenomenon can be used for improved interface reaction engineering, particularly in combination with RTP and particularly in gate stack technology [11]. However, the last thermal deuterium desorption peak is at around 550 °C which means that more stable passivation is expected.

Due to the fact that D adsorbs more strongly on Si surface than H, the D-passivation ensures a more robust technology for interface engineering than H-passivation [9,12]. A longer queue time is allowed between passivation and the following processing step. What is more, during the queue time a slightly elevated wafer temperature is allowed e.g. up to 60 °C. This helps to keep the passivated (hydrophobic) surface free from particles [13] and air borne organic depositions [14].

The purpose of this work is to demonstrate the effectiveness of the deuterium-passivation of the silicon surface, mainly by surface voltage and surface photovoltage methods.

2. Experimental

2.1. Sample preparation

Si single-crystal and porous Si (PS) layers were processed, since the high specific surface area of PS (200–600 m^2/g) facilitates the determination of the Si–H and Si–D bonds by infrared (IR) spectroscopy. Note that the inner surface of PS has nanoscaled crystalline planes of various directions. PS layer of 60% porosity and 10 μm thickness have been formed on Si substrate by dark anodization process.

In order to produce a vapor mixture of HF and water or heavy water, we designed and built a simple device as depicted in Fig. 1. The sample holder, including the Si wafer, was purged with N_2 to remove the air from the container. Nitrogen as a carrier gas was introduced into the bottle of HF and water/heavy water mixture. After the saturated gas mixture was formed above the liquid, the selected gas mixtures were introduced into the sample holder. The Si samples were treated for 1 min at 65 °C. The whole experimental setup, including the Si sample, was kept at the same temperature during the chemical treatment.

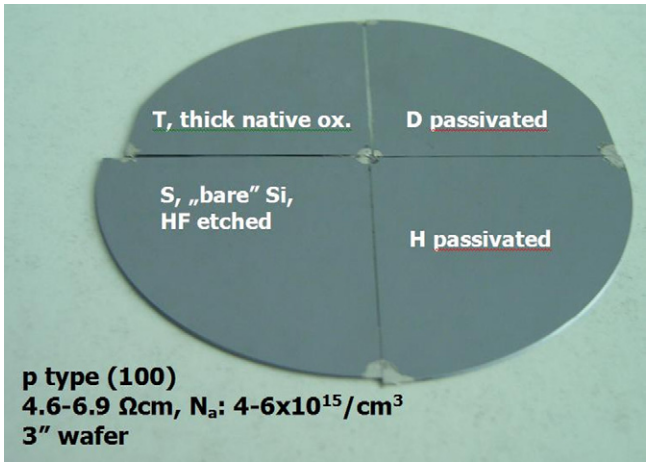

Fig. 2. Photograph of the differently passivated wafer quarters for surface voltage and surface photovoltage mapping.

In order to compare the effect of our new passivation method to the traditional one, Si surface cleaned by using wet chemical etching of native oxide layer (see in Table 1.). The four samples with different treatments (T: old native oxide on the surface, D: deuterium treated, H: hydrogen treated, S: HF etched bare Si surface) were fitted together for scanning surface potential and surface photovoltage measurements, as it can be seen in Fig. 2.

2.2. Test methods for the evaluation of the surface passivation

The vapor phase H- and D-passivated Si surfaces were investigated by contact angle measurements, spectroscopic ellipsometry, atomic force microscopy, X-ray photoelectron spectroscopy and transmission electron microscopy. The porous silicon samples were treated by the same method (Fig. 1) and these were studied by infrared absorption spectroscopy [15]. In the case of simple silicon slices the surface region is too small compared to the total silicon volume to get enough information by the infrared absorption spectroscopy. The high surface to volume ratio of the PS model system resulted in a better infrared absorption signal to noise ratio.

2.3. Surface voltage and surface photovoltage: the theoretical background

The surface voltage is not well defined on the thin insulator (oxide) covered or passivated silicon without metal gate electrode. Assuming zero electric field above the surface, the surface voltage can be expressed with oxide (insulator) surface charge (Q) and the SiO_2–Si interface charge ($Q_{ss} = Q_f + Q_{it}$):

$$V = V_{ox} + \Psi - \Phi_{ms} = \frac{Qd_{ox}}{\varepsilon_{ox}} + \Psi(Q + Q_f + Q_{it}) - \Phi_{ms} \quad (1)$$

Table 1
Samples prepared for surface investigations, analysis and vibrating capacitor (Kelvin) measurements, designated as "H", "D", "S" and "T", respectively.

Samples and procedures	p-type (100), 4.6–6.9 Ωcm, 3″ wafer			
	H-passivated	D-passivated	S "bare" Si	T thick native ox.
1. Step: cutting	One quarter of 3″ wafer	One quarter of 3″ wafer	One quarter of 3″ wafer	One quarter of 3″ wafer
2. Step: cleaning	100% HNO_3 at RT, 5 min; rinse in DI water; dry in N_2	100% HNO_3 at RT, 5 min; rinse in DI water; dry in N_2	100% HNO_3 at RT, 5 min; rinse in DI water; dry in N_2	100% HNO_3 at RT, 5 min; rinse in DI water; dry in N_2
3. Step: vapor phase treatment	1:20 = HF:H_2O + $(CH_3)_2CHOH$ at 65 °C, 1 min; rinse in H_2O (DI); dry in N_2	1:20 = HF:D_2O + $(CH_3)_2CHOH$ at 65 °C, 1 min; rinse in D_2O (99,8%) dry in N_2	1:20 = HF:H_2O at RT, 1 min; rinse in H_2O (DI); dry in N_2	No treatment, native oxide exists on the surface
4. Step: storage	in N_2	in N_2	in N_2	in N_2