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Effects of Si doping on the structural and electrical properties of Ge₂Sb₂Te₅ films for phase change random access memory

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Abstract

The effects of Si doping on the structural and electrical properties of $Ge_2Sb_2Te_5$ film are studied in detail. Electrical properties and thermal stability can be improved by doping small amount of Si in the $Ge_2Sb_2Te_5$ film. The addition of Si in the $Ge_2Sb_2Te_5$ film results in the increase of both crystallization temperature and phase-transition temperature from face-centered cubic (fcc) phase to hexagonal (hex) phase, however, decreases the melting point slightly. The crystallization activation energy reaches a maximum at 4.1 at.% and then decreases with increasing dopant concentration. The electrical conduction activation energy increases with the dopant concentration, which may be attributed to the increase of strong covalent bonds in the film. The resistivity of $Ge_2Sb_2Te_5$ film shows a significant increase with Si doping. When doping 11.8 at.% of Si in the film, the resistivity after 460 °C annealing increases from 1 to 11 m\Omega cm compared to the undoped $Ge_2Sb_2Te_5$ film. Current–voltage (*I–V*) characteristics show Si doping may increase the dynamic resistance, which is helpful to writing current reduction of phase-change random access memory.

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1. Introduction

As electronic portable and multimedia markets rapidly expand, there is a growing demand for nonvolatile memory with such good characteristics as small cell size, high density, low cost, and high endurance. Flash memory technologies based on the floating gate, the most extensive nonvolatile memory, are increasingly challenged to downscaling beyond 65 nm node [1], novel alternative nonvolatile memory technologies are being actively investigated. Among the next-generation memory technologies, phase-change random access memory (PRAM) has recently been regarded as the most promising universal nonvolatile memories due to its fast write/ read speed, high endurance, high scalability and good compatibility with CMOS technologies [2–5].

PRAM relies on the rapid reversible phase change between amorphous and crystalline states induced by the electrical current pulse in the $Ge_2Sb_2Te_5$ film, which is commonly used in commercially available re-writeable CD and DVD disks [6]. By applying a low and a bit longer current pulse a small volume of GST film is heated at the temperature between the crystallization temperature and melting point and form the crystalline state. To drive the film from the crystalline state to amorphous state, a small portion of the film must be heated above the melting point by a high and short current pulse and rapidly quench in the amorphous state. Currently, one of the main obstacles for downscaling PRAM is high current required for amorphization process, the so-called writing current. In order to develop high density PRAM, writing current must be reduced to match the current limit of drive transistors [7]. Among several

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solutions, it has been demonstrated that increasing the crystalline resistance of $Ge_2Sb_2Te_5$ film is a very effective way for reducing writing current [8–10]. In this paper, we firstly try to improve the electrical properties by doping Si in the $Ge_2Sb_2Te_5$ film. The Si doping effects on the electrical and structural properties of the $Ge_2Sb_2Te_5$ film are investigated in detail.

2. Experimental details

The 230-nm-thick Si-doped Ge₂Sb₂Te₅ film was cosputtered on SiO₂/Si (1 0 0) wafer with Ge₂Sb₂Te₅ alloy and Si targets in ULVAC MPS-3000 ultrahigh vacuum magnetron sputtering apparatus. The background pressure was below 3×10^{-5} Pa and the sputtering pressure is 0.2 Pa. Sputtering power of Ge₂Sb₂Te₅ target was 60 W while the power of Si target was varied from 20 to 68 W for controlling Si concentration in the film.

The chemical composition of the film was determined by Xray photoelectron spectroscopy (XPS). The as-deposited films were annealed for 10 min at various temperatures in a protective Ar atmosphere. Differential scanning calorimetry (DSC) was employed to determine the crystallization temperature and melting point at the heating rate of 10, 20 and 30 °C/min, respectively. The crystal structure of the annealed film was identified by X-ray diffraction (XRD) analyses using Rigaku D/MAX 2550 V diffractometer. The sheet resistance of film was measured with four-point probe technique. The electrical conductivity of the film in the temperature range of 303–373 K was measured in sandwich configuration using W electrodes. The temperature was accurately controlled using AL808 temperature controller. *I*–*V* characteristics of thin films were investigated using semiconductor parameter analyzer (Agilent 4156C) in the device structure and test circuit as shown in Fig. 1. A protective load resistor $R_{\rm L}$ was placed in series with the device and *I*–*V* characteristic was obtained by increasing the voltage ($V_{\rm Applied}$) stepwise and measuring the device voltage ($V_{\rm Device}$) and current at each step.

3. Results and discussion

3.1. Structural properties

Fig. 2 shows the XRD patterns of undoped and Si-doped Ge₂Sb₂Te₅ films annealed for 10 min at various temperatures in Ar gas. From Fig. 2(a), the crystal structure of Ge₂Sb₂Te₅ shows fcc structure and the lattice parameter is 0.5964 nm, which is slightly smaller than that reported in previous literature [11]. The reason is that the annealing temperature is 260 °C in our work but 170 °C in literature [11] and higher annealing temperature may result in the decrease of lattice parameters. As the dopant concentration increase, the intensity of fcc peaks decrease. When the dopant concentration increases to 11.8 at.%, no clear diffraction peaks appear in XRD pattern, which indicate it still remains amorphous. It can be deduced that the crystallization temperature increases due to Si doping. After annealed at 460 °C, the Ge₂Sb₂Te₅ film has been transformed from fcc to hex phase, as shown in Fig. 2(b). When the dopant concentration is below 7.2 at.%, the film



Fig. 1. (a) Schematic structure of the device in the I-V measurement and (b) test circuit used to investigate electrical properties of the device.

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