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Stress-induced leakage currents of the RF sputtered Ta_2O_5 on N-implanted silicon

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Abstract

The electrical (*C–V* and *I–V*) and reliability (constant current stress technique) properties of RF sputtered 30 nm thick Ta_2O_5 on N-implanted Si have been investigated. The dependence on the parameters of both Ta_2O_5 and the implanted interfacial layers on the stress time are discussed. The leakage current characteristics are analyzed by previously proposed comprehensive model. It is established that the reliability of the Ta_2O_5-based capacitors can be effectively improved if the Si substrate is a subject to preliminary N-implantation—markedly smaller stress induced leakage current as compared to the films on bare Si are detected. The stress mainly affects the properties of the interfacial layer and the generation of neutral traps is identified to be the primary cause for the stress-induced degradation. It is concluded that the implantation results in a strengthening of the interfacial layer against stress degradation.

Keywords: Constant current stress; Tantalum pentoxide; N-implantation; Silicon

1. Introduction

Ta_2O_5 with its high dielectric constant (≥25), low leakage current ($\leq 10^{-8}$ A/cm^2) and relatively high breakdown field (2–4 MV/cm) is one of the best high permittivity (high-*k*) dielectric-candidates to replace SiO_2 and SiO_xN_y in high density (nano-scale) dynamic random access memories (DRAMs) [1]. A number of methods compatible with silicon technology are successfully developed for obtaining thin films Ta_2O_5 [2–9]. During the formation of Ta_2O_5 on Si, however, an interfacial SiO_2-containing layer is inevitably formed at the Si substrate [9–16]. The growth of this layer is related with the known thermodynamical instability of the most high-*k* materials in direct contact with Si against formation of SiO_2 (Ta_2O_5 is not an exception). The precise description of the behavior of high-*k* dielectrics requires considering them as stacked high-*k*/interfacial layer structures. The thickness and the composition of thin interfacial lower-*k* layer depend strongly on the technological history of the system Ta_2O_5/Si (including all annealing steps), and consequently are a subject of a great debate and ongoing investigations [2,5,9,13,15,17–22]. Our structural studies of both RF sputtered and thermally grown Ta_2O_5 have shown that the interfacial layer is composed of ultrathin SiO_2 and a near interfacial region containing Ta- and Si-suboxides [12,13]. We have also reported that the dielectric and electrical characteristics of the Ta_2O_5/Si structures can be improved by annealing in O_2 or N_2 [14–16], and this is due to the better microstructure and stoichiometry of both the bulk Ta_2O_5 and the interfacial layer including reduction of its thickness after annealing. Nevertheless the low dielectric constant of this interfacial layer compromises the benefits of Ta_2O_5 as a high-*k* material and limits the minimal achievable equivalent oxide thickness. As far as this layer controls the leakage current through the stacked film a suppression of its undesirable impact on the global dielectric constant is necessary. A possible way to minimize (even to prevent) the growth of SiO_2-containing interfacial layer is a slight nitridation of Si before deposition of Ta_2O_5 resulting to formation in fact of SiO_xN_y at the Si instead of SiO_2 [22–24]. SiO_xN_y is not only with higher *k* than SiO_2, but it is expected to improve the reliability and immunity of the stack capacitor to hot electron degradation [25,26]. Among a number

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of methods for Si surface nitridation we used N-implantation in this work. The aim of the paper is to study the electrical and reliability properties of the capacitors based on RF sputtered Ta_2O_5 on nitrided Si. By using the comprehensive model [18] for the leakage current at both gate polarities, the parameters of Ta_2O_5 and the implanted layer are determined, and their dependence on the stress time are discussed.

2. Experimental

Chemically cleaned n-type (1 0 0) Si substrates with resistivity 4 Ω cm were implanted with nitrogen ions with energy of 1 keV and a dose of 3×10^{16} cm^{-2} by plasma immersion implantation. The penetration depth of N^+ was about 4 nm. After the ion implantation tantalum pentoxide thin film with a thickness of 30 nm was deposited by a reactive sputtering of Ta target in a mixture of 10% O_2 and Ar. The total pressure during the deposition was 3.3 Pa; the RF power density was 3.6 W/cm^2; Si substrate was heated at 220 °C. Details on the deposition can be found elsewhere [13]. It was expected that as a result of nitrogen ion implantation and subsequent Ta_2O_5 deposition a thin oxynitride layer or a mixed Si_3N_4-like/SiO_xN_y one at the Si interface is formed. The thickness d and the refractive index n of the film were measured ellipsometrically (λ = 632.8 nm). The refractive index n is found to be 2.1, which is the typical value for Ta_2O_5. No annealing steps were performed after nitridation of Si or Ta_2O_5 deposition.

Al gate metal-insulator-Si (MIS) capacitors were used as test structures for electrical characterisation of the films. The top Al electrode was evaporated and structured by photolithography to form capacitors with gate areas of 2.5×10^{-3} cm^2. Post-metallization annealing (PMA) was performed at 450 °C for 1 h in H_2.

The capacitance–voltage, *C–V*, curves were measured at 1 MHz (HP 3284 A LCR meter) and the effective dielectric constant ε_{eff} of the layers was determined from the capacitance value C_{ac} at accumulation using the measured thickness of the stacked film (d = 34 nm). The leakage currents and conduction mechanisms in the structures were evaluated by measuring *I–V* curves before and after constant current stress. *I–V* characteristics were obtained by using a HP 4140 A picoampermeter/dc voltage source, for both positive and negative gate polarity. Current was measured in steps of 0.1 V, with a hold time of 5 s, allowing obtaining negligible displacement current. Constant current stresses for total stress times of 11, 96, 995 and 4068 s at the current density of 10 mA/cm^2 were performed. The stress time values were so chosen to form approximately a geometric progression, thus covering many orders of magnitude with small number of points, because the measurements of *I–V* characteristics as well as their analyses are highly time consuming.

3. Results and discussion

The *C–V* curves were measured only in the range from −2 to 2 V, because at higher voltages the leakage currents become important and could affect the measurement. In order to determine the value of the capacitance of ultrathin high-k dielectric, the method of extraction described in Refs. [27,28] was used. Thus obtained value of the capacitance in accumulation was C_{ac} = 855 pF. By applying standard procedures for MIS structures, the equivalent oxide thickness d_{eq} = 10.09 nm (*i.e.* the thickness of a SiO_2 layer that would give the same value C_{ac}), the effective dielectric constant ε_{eff} = 13.1, the flatband voltage $V_{fb} = -0.18$ V and the oxide charge density in the insulating film $Q_f = 2.4 \times 10^{11}$ cm^{-2} were determined. A typical feature of the high-k dielectrics is the hysteresis observed in the *C–V* curves when reversing the direction of sweeping (Fig. 1). The flatband voltage shift (ΔV_{fb}) between the two curves is about 90 mV, and respectively the density Q_{it} of the slow states evaluated from ΔV_{fb} is 1.9×10^{11} cm^{-2}.

Leakage current at a given applied voltage is a crucial parameter describing insulating films obtained at certain technological parameters. Besides, the measurement of the *I–V* characteristics allows elucidating conduction mechanisms and extracting some important parameters of the layers. Stress-induced leakage currents (SILC) are important from the reliability point of view when studying the degradation of the insulating films during high-field/current stress.

Leakage currents increase with the stress time for both polarities (Fig. 2). This effect is less clearly visible for the negative bias due to the saturation above 1.5 V. Detailed analysis of these results will be done in terms of the comprehensive model presented in Ref. [18] that we applied in Refs. [3,8].

We consider the insulating film to be composed of two layers, starting from the Si substrate: silicon nitride (SN) and Ta_2O_5 (tp). It is expected the layer obtained by implantation without annealing can be treated roughly as a homogeneous Si_3N_4-like layer (SiN_x). The appearance of a transition region between Ta_2O_5 and SiN_x can somehow modify the results obtained for the stacked layer SiN_x/Ta_2O_5. Therefore, the parameters extracted below have to be treated as effective values for the interfacial layer composed of the SiN_x part and

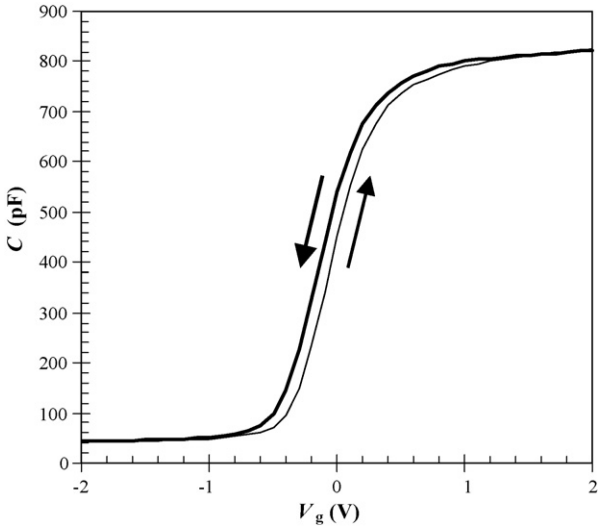

Fig. 1. High frequency (1 MHz) *C–V* hysteresis loops: the voltage is first swept from the right to the left (bold line) then back (thin line).