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Effect of interface traps on Debye thickness semiconductor films

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Abstract

The presence of the boundary interface trapping states and their role in determining the properties of Debye thickness thin semiconductor films, are demonstrated experimentally, using PbTe films deposited on mica. These charged states could not be observed earlier and be studied directly, because of the screening by the relatively high carrier density of the ordinary PbTe. Thin, Debye length thickness, PbTe films with a high concentration of interface trapping centers, possess an extraordinary high resistance. In this case the thermostimulated capacitor discharge method can be successfully applied to determine the energy of these levels, their carrier capture cross-sections and their donor- or acceptor-like character. The experimental results and theoretical calculations are discussed.
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1. Introduction

Recently [1] we described shortly the properties of unusually highly-resistive p-PbTe films deposited on mica substrates. We have also presented the arguments that the condition to obtain such highly-resistive films requires a sufficiently large density of carrier trapping centers at the substrate–PbTe interface, so that free carriers will be drained, almost completely, from an interface layer of a thickness close to the Debye screening length L_S. (For PbTe with typical doping $\sim 10^{17}\ \mathrm{cm}^{-3}$ the value of $L_S \approx 500$ Å.) Then, a film with the thickness $L \approx L_S$, becomes highly-resistive. It should be emphasized that these conditions are quite general, and are not limited to a particular combination of semiconductor/substrate or on the method of

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preparation, as long as the density of the trapping states is adequate and the film thickness is of the order of Debye screening length.

We have shown that the free carrier concentration in these films can be as low as $\sim 10^{14}\,\mathrm{cm}^{-3}$ at a temperature of $T \approx 100$ K, i.e. the carrier concentration is close to the intrinsic. Such high resistance films, having an extraordinary low concentration of free carriers, allow to investigate a whole series of phenomena in the $A^{IV}B^{VI}$-semiconductors, such as injection currents, injection electroluminescence, electronic memory phenomena, electric field effect control of thermopower and more.

The objective of the current work was to demonstrate, by direct measurement, the presence of the interface states in the mica–PbTe structure, and to determine their energies, capture cross-sections and their (donor or acceptor) nature. Owing to the high electrical resistance of the sample, we found as most suitable to achieve these objectives the thermoactivation method [2], in particular, the method of the thermostimulated capacitor discharge (TSCD) [3,4].

2. The TSCD method

The TSCD method is illustrated in Fig. 1, where the experimental Metal-Dielectric-Semiconductor (MDS) sample structure and the measurement circuitries are drawn schematically.

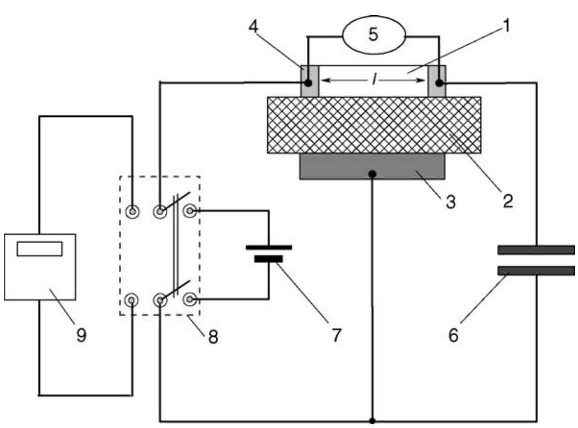

Fig. 1. The schematics of the TSCD method with the auxiliary capacitor. (1) PbTe film; (2) mica; (3) gate; (4) contacts to PbTe; (5) electrostatic electrometer measuring ΔV; (6) the auxiliary capacitor C_{ad}; (7) high voltage source; (8) electrical polarity switch key; (9) electrometer measuring the discharge current I.

2.1. The field-cooled (FC) process

The measurement procedure of the standard TSCD method [3,4], consists of the following:

(1) The semiconductor layer is charged (positively or negatively) by the gate voltage V_g, at an elevated temperature. Thus, the p-PbTe capacitor plate acquires an electrical charge of $Q_g = CV_g$, where C is the capacitance of the MDS structure.
(2) Then, the sample is cooled slowly, under the voltage V_g, to a lower temperature T_0. During this period, the occupation of the localized centers in the film occurs under, practically, equilibrium conditions. If T_0 is sufficiently low, the majority of the injected charges are captured by the localized levels, leaving only a small fraction as free carriers.
(3) Then, the charged sample and the gate are shortened trough the electrometer, and the free carriers leave the semiconductor plate for the metal gate. Due to the remaining induced charge, captured at the localized centers, the RC time constant of the sample capacitive structure is very high [5].
(4) The temperature of the film is then increased at a constant heating rate β, i.e. $T = T_0 + \beta t$, where t is the time.
(5) With increasing temperature, the carrier life-time on the trap decreases, and levels, having the appropriate energy E_i, will be emptied. The carriers captured on these levels will be excited to the corresponding band, and then leave the sample film for the gate, flowing through the electrometer. Thus, the carriers, excited from the E_i energy traps, will give at a certain temperature $T_{mi}(E_i)$ a maximum of the discharge current I_{mi}.

The kinetics of the discharge current, i.e. the function $I[T(t)]$ contains the information on the level parameters. The positions of the temperature maxima T_{mi} and the temperatures of their half-width points T_L (left) or T_R (right), allow, in principle, to determine the energies E_i of the traps and their capture cross-sections Σ_i.

The standard sensitivity of the TSCD method and its resolution capability (separation of the current peaks, belonging to different traps, on the $I(T)$-curve) are significantly improved [4] upon using an additional, auxiliary capacitor C_{ad} (see Fig. 1) with a much

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