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Fabrication and simulation of organic transistors and functional circuits

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ABSTRACT

We report the development of a vacuum-evaporation route for the roll-to-roll fabrication of functioning organic circuits. A number of key findings and observations are highlighted which influenced the eventual fabrication protocol adopted. Initially, the role of interface roughness in determining carrier mobility in thin film transistors (TFTs) is investigated. Then it is shown that TFT yield is higher for devices fabricated on a flash-evaporated-plasma-polymerised tri(propyleneglycol) diacrylate (TPGDA) gate dielectric than for TFTs based on a spin-coated polystyrene (PS) dielectric. However, a degradation in mobility is observed which is attributed to the highly polar TPGDA surface. It is shown that high mobility, low gate-leakage currents and excellent stability are restored when the surface of TPGDA was buffered with a thin, spin-coated PS film. The resulting baseline process allowed arrays of functional circuits such as ring oscillators, NOR/NAND logic gates and S–R latches to be fabricated with high yield and their performance to be simulated.

1. Introduction

The most widely adopted approaches for the roll-to-roll (R2R) fabrication of organic electronic devices and circuits are generally based on solution processing e.g. inkjet [1–3] and gravure [4–7] printing which have also been used in combination with other methods including screen and flexo printing [8,9]. However, devices fabricated using only solution processing can suffer from poor yield arising mainly from a defective gate insulating layer and layer interdiffusion. Open- or short-circuited electrodes and tracks can also become issues as device sizes are reduced and production speeds increase. The best performing organic circuits to date, however, have been achieved by combining solution processing with a photolithographic step [10–13]. The latter allows much higher resolution features to be formed which is especially important for defining the source–drain gap (channel length, L) in thin film transistors (TFTs). However, incorporating a photolithographic step into a roll-to-roll process is not trivial.

Given these problems and limitations, it is surprising perhaps that only limited interest has been shown in developing a fabrication method based on the vacuum-evaporation of all the device layers – metal, insulator and semiconductor. Such an approach overcomes many of the problems associated with solution processing. It is usually argued that the capital cost is prohibitive, yet commercial equipment is already available for (a) producing high resolution metal patterns on plastic sheets in a R2R process [14,15] and (b) depositing organic and inorganic barrier layers onto moving plastic webs [15–17] – in both cases by evaporation under vacuum.

We reported on the feasibility of a vacuum-evaporation route for organic thin film transistor (OTFT) fabrication some years ago [17]. The key step in the process was the production of the gate insulator in a vacuum R2R environment by deposition and subsequent electron-beam polymerisation of the deposited monomer tri(propyleneglycol) diacrylate (TPGDA). In this early work, the hole mobility in bottom-gate top-contact (BGTC) pentacene OTFTs was only ~0.09 cm^2/V s and the characteristics tended to be unstable. Also, pentacene is prone to long-term oxidative degradation so that identification of a high mobility, air-stable replacement semiconductor was essential. Although not reported earlier, top-gate bottom-contact (TGBC) OTFTs were also fabricated but showed much poorer performance. At the time, this was thought likely to be due to degradation of the pentacene by the high energy electron-beam used to polymerise the TPGDA.

In the following, previously unpublished results and data are used to trace, from this modest beginning, the development of a high-yield, baseline vacuum-evaporation process for the

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production of OTFTs with reproducibly good performance [18,19] which in turn has allowed the demonstration of functioning circuits [20].

2. Materials and methods

Dinaphtho[2,3-b:2′,3′-f] thieno[3,2-b]thiophene (DNTT) was chosen for this work since it has a similar mobility to pentacene but with better environmental stability [21] due to a reduced tendency to oxidise. It was synthesised following a previously published route [22] from 2-naphthaldehyde with 35% overall yield. By repetition of 300 mg scale iodine-catalysed ring closure followed by two recrystallisations from *o*-dichlorobenzene, high purity DNTT was obtained as bright yellow microcrystals in 1 g batches. TPGDA monomer and polystyrene (M_W = 350,000) were purchased from Sigma Aldrich and used without further purification.

Arrays of TFTs and circuits were fabricated on precleaned, 5 cm × 5 cm, 125 μm thick polyethylene naphthalate (PEN) substrates (Dupont-Teijin). Full details of our vacuum-fabrication procedures have been given in previous publications [17–19,23]. Briefly, aluminium gate electrodes and associated tracks were vacuum evaporated onto the substrates through shadow masks. Subsequently, the substrates were attached to a cooled web-coater drum (Aerre Machines). With the drum rotating at a linear speed of 25 m/min under vacuum, flash-evaporated TPGDA monomer vapour which condensed onto the substrates was cross-linked by exposure, in situ, to a plasma. The resulting smooth, pinhole-free films were typically 500 nm to 1 μm thick with a measured dielectric constant varying in the range 4–5. For circuit fabrication, the insulator was patterned using shadow masks to define rectangular areas separated by 1 mm gaps to act as vias for inter-layer metallic connections. The substrates were then transferred into an evaporator (Minispectros, Kurt Lesker) integrated into a nitrogen glovebox for the vacuum-deposition (2.4 nm/min) of DNTT onto the insulator. Without exposing the substrates to ambient air, the gold source/drain metallisation layer was deposited through a shadow mask in the same evaporator.

The OTFT masks defined an 18 × 5 array of 90 transistors with 5 capacitors arranged diagonally across the substrate. These capacitors were used to extract values for the capacitance per unit area of the gate dielectric for later use in parameter extraction. The variation in values over the substrate was typically less than 5%. The channel length L of the OTFTs in each row increased in steps from 50 to 200 μm. Each row comprised of two blocks of 9 OTFTs. In the left hand blocks the channel width, W, was 2 mm, yielding W/L ratios ranging from 40 in the first row down to 10 in the fifth row. In the right hand blocks of 9 OTFTs, a constant W/L ratio of 20 was maintained so that W ranged from 1 mm in the first row to 4 mm in the fifth row. Arrays of logic gates and ring oscillators were prepared on other PEN substrates using the fabrication protocols developed for the OTFTs [18,20]. Our OTFT designs were not optimised in the sense that allowances were made both for the resolution and registration ability (±100 μm) likely in a high-speed R2R process. The former limits channel length to ~40 μm, while the latter leads to the possibility of parasitic currents and capacitances in our devices and circuits as discussed later.

To counter the deleterious effects that the high-polarity TPGDA dielectric had on OTFT characteristics, it was found beneficial to passivate the insulator surface with thin (30–300 nm) polystyrene films (dielectric constant, 2.6) prior to depositing the semiconductor [24]. This was achieved by spin-coating from a toluene solution in a nitrogen glovebox and heating on a hot plate at 100 °C for 10 min. Also, for comparing the performances of top-gate versus bottom-gate OTFTs and process yield, some OTFT arrays were fabricated using thicker (~1 μm) spin-coated layers of polystyrene as the gate insulator.

Topographic images of the various film layers were obtained in tapping mode using a Veeco Dimension 3100 Atomic Force Microscope (AFM). OTFT characteristics were measured in air using a Keithley model 4200 Semiconductor Characterisation System in ambient dark conditions. Inverter transfer characteristics were obtained using the same system. The time responses of logic gates and ring oscillators were recorded by connecting the output of each circuit to a digital oscilloscope (Agilent DSO-X 2014A) via a buffer amplifier to minimise oscilloscope loading effects on the circuits. Device parameter extraction and circuit simulations were undertaken using Silvaco's Universal Organic Thin Film Transistor (UOTFT) Model (Level = 37) and Smartspice Circuit Simulator.

3. Results and discussion

3.1. Bottom-gate versus top-gate OTFTs

Our initial investigations into the use of vacuum-deposited TPGDA as a gate insulator had established that bottom-gate, top-contact (BGTC) pentacene TFTs, Fig. 1(a), were superior to top-gate, bottom-contact (TGBC) devices, Fig. 1(b). Since, the BGTC structure is simply the inverted form of the TGBC structure, significant differences in injection area at the source contact may be ruled out as the cause. It was thought initially that the difference arose from the detrimental effect of electron-beam or plasma processing of the insulator when overlying the semiconductor in the top-gate structures. To rule out such radiation-related effects, initial measurements on DNTT devices were made using spin-coated polystyrene (PS) as the gate insulator in BGTC and TGBC TFTs.

In Fig. 2 is shown the output (I_D vs V_D) and transfer (log I_D vs V_G) characteristics of a typical PS-based TGBC DNTT OTFT. The inset in Fig. 2(b) shows the gate-voltage dependence of the device mobility, μ, extracted in the linear regime using the equation

$$\mu_{lin} = \frac{\partial I_D}{\partial V_G} \cdot \frac{L}{WC_i V_D} \tag{1}$$

and in saturation using

$$\mu_{sat} = \left(\frac{\partial \sqrt{I_D}}{\partial V_G}\right)^2 \cdot \frac{2L}{WC_i} \tag{2}$$

where C_i is the capacitance per unit area of the gate dielectric layer.

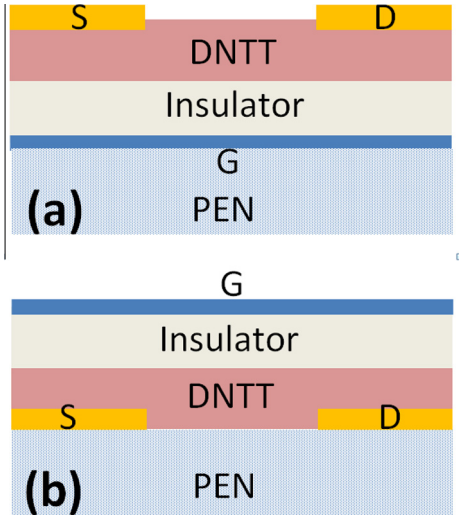

Fig. 1. Cross-sectional diagram of (a) bottom-gate top-contact (BGTC) and (b) top-gate bottom-contact (TGBC) on a PEN substrate.