Displays 44 (2016) 1–4

Contents lists available at ScienceDirect

Displays

journal homepage: www.elsevier.com/locate/displa

A LTPS-TFT pixel circuit for active matrix organic light emitting diode based on improved current mirror ☆

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ARTICLE INFO

Article history:
Received 20 August 2015
Received in revised form 9 November 2015
Accepted 22 May 2016
Available online 24 May 2016

Keywords:
Active matrix organic light emitting diode (AMOLED)
Low-temperature poly-silicon thin-film transistor (LTPS-TFT)
Current programmed pixel circuit (CPPC)
Channel length modulation effect

ABSTRACT

In this paper, a voltage-driving and current compensation method for active matrix organic light emitting diode (AMOLED) displays is proposed. An improved current mirror is introduced into the pixel circuit to overcome the channel length modulation effect of TFTs. The SPICE simulation results show that the proposed pixel circuit not only effectively compensates for non-idealities related with deviations of μ and V_T in TFTs, the OLED degradation, but also offers a less setting time and guarantees a good liner relationship between V_{DATA} and I_{OLED}.

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1. Introduction

Organic light-emitting diode (OLED) displays are one important type of self light-emitting display techniques. They offer many unique performances compared with liquid crystal displays (LCD), such as high contrast ratio, very fast response time (μs), wide diverging angle, and lower power-consumption. These merits make OLED display panels have great potentials for developing glass-free three-dimensional (3D) display techniques. At present, more and more television manufacturers begin to incorporate 3D display functions in their products. Due to the compatibility with existing plane image systems based on flat two-dimensional (2D) display panels [1], multi-view 3D display technologies become prosperous. Through presenting position dependent views of a 3D scene to viewers, the multi-view display can offer both stereo and motion parallax depth cues. Recently, taking advantages of wide diverging angles of OLED pixels, Teng et al. [2–4] solved the discontinuous motion parallax problem of multi-view 3D display systems. In general, high-refresh-rate and high-resolution AMOLED display panels are crucial for obtaining better 3D effects. Thus, low temperature poly-silicon thin film transistors (LTPS-TFT) have attracted wide attentions for AMOLEDs, due to their higher field-effect mobility and better electrical stability compared to other TFT technologies.

However, random distribution of grain boundaries in poly-silicon films cause the inevitable non-uniformity of LTPS-TFT parameters, including mobility (μ) and threshold voltage (V_T) [5]. The application of LTPS-TFTs in flexible displays poses an additional stress factor to AMOLEDs, which will also result in non-uniformity varied with deformation. In addition, the threshold voltage of OLEDs (V_{T_OLED}) degrades at 0.2 mV/h during operation [6]. The conventional pixel circuit of two transistors and one capacitor (2T1C), as shown in Fig. 1(a), doesn't work for the non-uniformity of AMOLED display panels. As a result, some compensation methods have been proposed [5–14]. In those methods, voltage compensation has a faster setting time, but at the price of less effective compensation for V_{TH} shift than the current compensation scheme [10]. However, the current compensation methods require inconvenient constant current sources [8], and ignore the channel length modulation effect of TFTs [15]. A typical mirrored current programmed pixel circuit (CPPC) is shown in Fig. 1(b) [7].

In this work, an improved current mirror pixel circuit is proposed which uses voltage driving and provides current compensation. The compensation circuit takes the advantage of current compensation and avoids the disadvantage of using constant

☆ This paper was recommended for publication by Pen-Cheng Wang.

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http://dx.doi.org/10.1016/j.displa.2016.05.005
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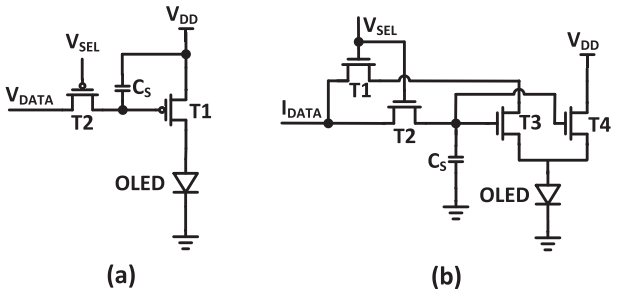

Fig. 1. (a) The conventional 2T1C pixel circuit, (b) the typical mirrored current programmed pixel circuit (CPPC).

current sources. The improved current mirror can make the input voltage (V_{DD}) and the output current (I_{OLED}) exhibit a good linear relationship by overcoming the channel length modulation. As a result, the pixel circuit not only can effective compensate μ and V_T shifts of TFTs, the OLED degradation, but also offers a less setting time.

2. Proposed pixel circuit and driving method

The proposed pixel circuit is schematically drawn in Fig. 2(a), which includes six P-type TFTs (T1-T6) and one storage capacitor (C_S). The column external driver circuit consists of an integral module and a current sensing module [11]. Signal communications between the pixel circuit and the external driver are carried out through the data line and the feedback line.

The signal timing diagram is given in Fig. 2(b). The operation consists two phases: programming model and hold model. During the programming model, V_{SEL} is low to turn on T1 and T2, the output voltage of AMP_1 (V_{FB}) is given as:

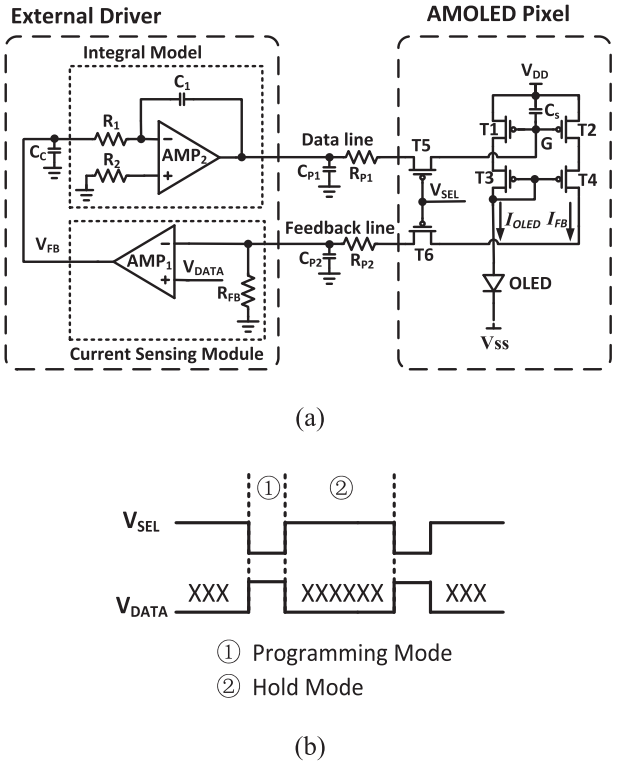

Fig. 2. (a) Equivalent circuit of the proposed driving scheme, (b) signal timing diagram.

$$V_{FB} = (V_{DATA} - I_{FB} \times R_{FB}) \times G \tag{1}$$

where G is the gain of the amplifier (AMP_1).

The output voltage (V_{OUT}) of the integral module is derived by integrating V_{FB}:

$$V_{OUT}(t_2) = -\frac{1}{R_1 C_1}\int_{t_1}^{t_2} V_{FB}dt + V_{OUT}(t_1) \tag{2}$$

where $V_{OUT}(t_1)$ and $V_{OUT}(t_2)$ are the voltage values of V_{OUT} at the start time of t_1 and the end time of t_2, R_1 and C_1 denote the values of the used resistor and capacitor.

The channel length modulation effect of TFT will make the drain current (I_D) keep changing with the variation of V_{DS} in saturation region. In the proposed pixel circuit, this effect of TFT is taken into consideration by using the MOS model [16], the drain current of T1 and T2 in saturation region can be expressed as

$$I_D = \frac{1}{2}\mu C_{ox}\left(\frac{W}{L}\right)(V_{GS} - V_T)^2(1 + \lambda V_{DS}) \tag{3}$$

where C_{OX} denotes the gate capacitance, μ is the mobility, W/L denotes the aspect ratio of TFT. The threshold voltage V_T and the channel length modulation factor λ are introduced into the equation. Hence,

$$\frac{I_{D1}}{I_{D2}} = \frac{(W/L)_1}{(W/L)_2}\cdot\frac{(1 + \lambda V_{DS1})}{(1 + \lambda V_{DS2})} \tag{4}$$

Compared with the typical mirrored CPPC, the proposed pixel circuit adds two TFTs (T3 and T4) to cope with the channel length modulation effect. In this way, $V_{D1} + V_{SG3} = V_{D2} + V_{SG4}$. If $(W/L)_3/(W/L)_4 = (W/L)_1/(W/L)_2$, then $V_{SG3} = V_{SG4}$ and $V_{D1} = V_{D2}$. According to the device parameters summarized in Table 1, I_{OLED} and I_{FB} are equal.

At the end of programming mode, the improved current mirror pixel circuit takes the self-regulation voltage (V_G) through voltage driving and current feedback operation, the negative feedback system will keep balance, leading to:

$$I_{OLED} = I_{FB} = \frac{V_{DATA}}{R_{FB}} \tag{5}$$

Since I_{OLED} is determined by V_{DATA} and R_{FB}, the final stabilized I_{OLED} will be insensitive to variations of the electrical properties of TFTs and OLEDs. Thus, the proposed driving scheme has high immunity to the variation of LTPS-TFTs and OLED characteristics.

During the hold phase, V_{SEL} is high to turn off T1 and T2. Consequently, C_S continues to sustain V_G. Therefore, I_{OLED} will keep a specific value, the same as that at the end time of programming model.

3. Simulation setup

To verify performances of the proposed driving scheme, circuit simulations are conducted by the Cadence-virtuoso software. A p-type LTPS-TFT SPICE model (Level 62) is used, where μ and V_T are set as 48 cm^2/V s and −2.5 V, respectively. The output characteristics of the LTPS-TFTs are simulated, as shown in Fig. 3(a), which

Table 1
Device parameters used in the simulation.

TFT	W/L value	Capacitor	Value (pF)	Resistor	Value (kΩ)
T1	15 μm/5 μm	C_1	10	R_1	10
T2	15 μm/5 μm	C_C	5	R_2	1
T3	5 μm/5 μm	C_S	5	R_{FB}	10
T4	5 μm/5 μm	C_{P1}	100	R_{P1}	1.5
T5	5 μm/5 μm	C_{P2}	100	R_{P2}	1.5
T6	5 μm/5 μm				

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