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Single-layer obstacle-aware routing for substrate interconnections

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ABSTRACT

Due to the limit of available layers and the existence of obstacles in a routing region, single-layer obstacle-aware routing becomes an important issue for substrate interconnections. In this paper, based on the terminals of the given nets, the corner of the rectangular obstacles and the routing plane, routability-driven constrained Delaunay triangulation can be firstly constructed. Furthermore, based on the construction of routability-driven constrained Delaunay triangles, a flow-based approach is proposed to assign the global wires of the given nets in a single layer and an efficient approach is proposed to assign the physical paths of the given nets for single-layer obstacle-aware routing. Compared with the 97.35% routability of the routing nets in the modified combination of Liu's topological router [13] and our proposed detailed router for substrate routing with the rectangular obstacles, the experimental results show that our proposed flow-based approach can use less CPU time to obtain the 99.90% routability of the routing nets and shorter total wirelength in a single layer on the average for the tested examples.

1. Introduction

As the complexity increases and the feature size decreases in modern VLSI designs, the requirement of more IO pads becomes a critical issue. Recently, an IC package uses a ball grid array(BGA) substrate to connect a die with the wire-bonding or flip-chip interconnections to the substrate. However, the high-density integration in an IC package makes the off-chip interconnections difficult. For a wire-bonding die, the IO pads are connected to the corresponding bond pads through a set of bounding wires. On the other hand, an advanced packaging technology, *flip-chip(FC) package* [1], is introduced to meet the requirement of the higher integration density and the larger IO count in complicated VLSI circuits. Recently, the chip-package codesign can be divided into three sequential routing steps: *RDL routing*, *Escape routing* and *Substrate routing* as illustrated in Fig. 1. For a flip-chip die, an extra metal layer, *redistribution layer (RDL)*, is firstly used to redistribute the IO pads to the bump balls without changing the locations of the placed IO pads in RDL routing [2–6]. Furthermore, escape routing[7,8] breaks out all the bump pads to the chip boundary at the break pads in the given layers. Finally, a set of substrate interconnections from the bond pads in the wire-bonding dies or the break pads in the flip-chip dies to the solder balls in a BGA package must be connected in substrate layers for substrate routing [10–13].

In *pre-assignment* RDL routing, the IO connections between IO pads and bump balls have been assigned before routing. Hence, the solution in the *pre-assignment* problem depends on the assignment of the given IO connections. For *pre-assignment* RDL routing, some related works [2–5] were published. Fang et al. [2] addressed the pre-assignment problem with boundary-IO pads and presented an integer linear programming(ILP)-based approach to complete the global routing and an X-based gridless routing approach to complete the detailed routing in the redistribution layer. However, the proposed ILP formulation for the pre-assignment problem is too time-consuming. Based on the re-numbering technique of IO connections and the routable separation of four sectors in a flip-chip design, Yan et al. [3] also proposed an efficient routing approach to route all the IO connections in the pre-assignment problem with peripheral-IO pads. Fang et al. [4] also proposed an effective global router to improve the performance of their proposed ILP-based flip-chip global router in the pre-assignment problem with area-IO pads. Based on the extraction of the maximum net sequence, Yan et al. [5] also proposed an efficient routing approach to route all the IO connections in the pre-assignment problem with area-IO pads. However, the pre-assignment RDL routing problems with peripheral-IO or area-IO pads do not consider the obstacles and restrict the bump balls or IO pads to the pre-designed locations. Hence, the pre-assignment RDL routing problem belongs to a single-layer restricted routing problem.

For a given set of points in a two-dimensional(2D) plane, the most common and useful triangulation is the Delaunay triangulation. If there is a circle passing through a pair of two points so that the other points in a 2D plane lie outside the circle, the edge between the two points is an edge of the Delaunay triangulation. In Delaunay triangulation, all triangles have empty circumscribed circles, that is, no point lies in the interior of any triangle's circumcircle. Generally speaking, Delaunay triangulation in a 2D plane is unique if four points in a given set of points are not co-circular. To set some specified edges as the triangle edges in

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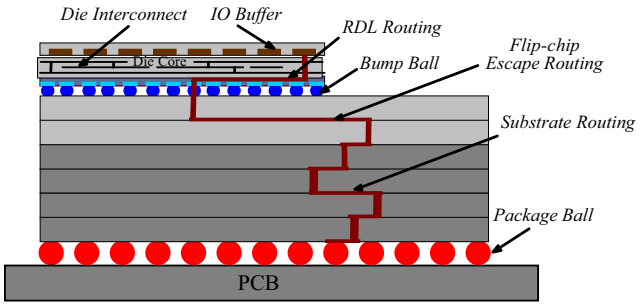

Fig. 1. Connection of an IO signal in chip-package codesign.

Delaunay triangulation, a modified version of the Delaunay triangulation, *constrained Delaunay triangulation* [9], can be considered to generate the constrained triangles with some user-defined specified edges. Based on the construction of a Manhattan Voronoi diagram in a routing plane, Yan et al. [6] proposed an efficient approach use the concept of Delaunary triangulation to assign all the IO connections onto the IO buffers in a routing plane for the RDL routing problem with area-IO pads.

For substrate interconnections, the routing concept was published in some related packages [10,11]. However, it is assumed that the bond pads or break pads in the published works are located side by side with respect to solder balls. Recently, Liu et al. [12,13] also developed an efficient yet effective algorithm for substrate topological routing. In the work, they explain why planar routing is still required with multiple routing layers for substrate routing and propose a flexible via-staggering technique to improve routability. However, the proposed approach does not consider the existence of obstacles for substrate routing. Due to the limit of planar routing and the existence of obstacles for substrate interconnections, single-layer obstacle-aware routing becomes an important issue for substrate interconnections.

The contributions of this paper can be summarized in the following:

(1) Given a set of two-terminal nets and a set of rectangular obstacles in a routing plane, based on the terminals of the given nets, the corner of the rectangular obstacles and the routing plane, routability-driven constrained Delaunay triangulation can be firstly constructed.
(2) Based on the construction of routability-driven constrained Delaunay triangles, a flow-based approach is proposed to assign the global wires of the given nets in a single layer and an efficient approach is further proposed to assign the physical paths of the given nets for single-layer obstacle-aware routing.
(3) Compared with the 97.35% routability of the routing nets in the modified combination of Liu's topological router [13] and our proposed detailed router for substrate routing with the rectangular obstacles, the experimental results show that our proposed flow-based approach can use less CPU time to obtain the 99.90% routability of the routing nets and shorter total wirelength in a single layer on the average for the tested examples.

The rest of this paper is organized as follows: Section 2 contains the problem formulation of single-layer obstacle-aware routing for substrate interconnections. Section 3 provides a flow-based approach to assign all the two-terminal nets with the crossing and obstacle constraints in a single routing layer. In Section 4, the experimental results for the proposed flow-based approach are listed and compared with the previous published approaches. Finally, the conclusions and further works are summarized in Section 5.

2. Problem formulation

In general, single-layer obstacle-aware routing for substrate interconnections is only allowed to route all the nets in a single routing layer. Hence, the *wire crossing* between any pair of nets cannot be allowed in the routing layer. Additionally, the *wire overlapping* between any net and any obstacle cannot be allowed in the routing layer. Hence, the *non-crossing constraints* in the given nets and the *non-overlapping constraints* between the given nets and obstacles must be maintained for single-layer obstacle-aware routing.

Given a set of n two-terminal nets, $N=\{N_1, N_2,\ldots, N_n\}$, and a set of m rectangular obstacles, $O=\{O_1, O_2,\ldots, O_m\}$, in a single-layer grid-based routing plane, it is assumed that $S=\{s_1, s_2,\ldots, s_n\}$ is a set of n start terminals and $T=\{t_1, t_2,\ldots, t_n\}$ is a set of n target terminals in N. It is assumed that the connection of any two-terminal net goes through the grid edges in a grid-based routing plane. Basically, any start terminal, s_i, $1 \le i \le n$, is connected to its corresponding target terminal, t_i, to form a two-terminal net, N_i, and the wirelength of the net, N_i, is defined as the number of the passing grid edges from the start terminal, s_i, to the target terminal, t_i. In single-layer grid-based routing model, any routing wire must be assigned onto a grid line. Hence, the single-layer obstacle-aware routing problem in a grid-based routing plane is to assign the routing wires of the given nets onto feasible grid edges to maximize the number of routed nets in a single routing layer with satisfying the non-crossing and non-overlapping constraints.

3. Single-layer obstacle-aware routing for substrate interconnections

Given a set of n two-terminal nets, $N=\{N_1, N_2,\ldots, N_n\}$, and a set of m rectangular obstacles, $O=\{O_1, O_2,\ldots, O_m\}$, in a single-layer grid-based routing plane, the routing process in single-layer obstacle-aware substrate routing can be divided into three phases: *Construction of routability-driven constrained Delaunay triangulation*, *Single-layer obstacle-aware global routing* and *Single-layer obstacle-aware detailed routing* and the design flow of the routing process can be shown in Fig. 2.

3.1. Construction of routability-driven constrained Delaunay triangulation

Based on the start and target terminals of the given nets and the corners of the rectangular obstacles and the routing plane, the

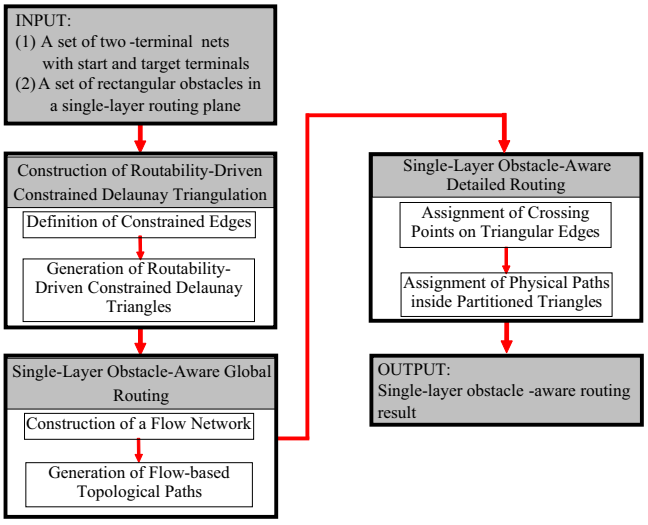

Fig. 2. Design flow in single-layer obstacle-aware routing.