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A new leakage-tolerant domino circuit using voltage-comparison for wide fan-in gates in deep sub-micron technology

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ABSTRACT

In this paper, a new leakage-tolerant domino circuit is presented which has lower power consumption and higher noise immunity without significant delay increment for wide fan-in gates. The main idea in the proposed circuit is using sense amplifier for sensing the difference between voltages across the pull down network (PDN). This strategy provides correct output. In the proposed technique, therefore, the voltage swing of the dynamic node can be reduced to decrease the power consumption caused by the heavy switching capacitance in wide fan-in gates. The simulation is provided with 64-bit wide OR gates using a 90 nm CMOS technology model. The simulation results are compared with that of standard domino circuits at the same delay, and 35% power consumption reduction and 2.31 × noise-immunity improvement are observed.

1. Introduction

Dynamic logics such as domino logic are widely used in many applications due to their potential advantages over static logics, especially in the high-speed data paths [1,2]. The main advantage of the dynamic logic includes its high speed and small chip area. In spite of these benefits, dynamic logic suffers from lower noise immunity and higher power consumption in comparison to the static logic. On the other hand, as the technology and the supply voltage are scaled down, the threshold voltage (V_{Th}) of the MOS devices should be reduced to mitigate speed loss. This condition exponentially increases the leakage current and results in higher static power dissipation as well as lower noise margin. Thus, improving noise immunity and reduction of leakage power are the main issues in noise immune and high performance designs in ultra deep sub-micron regime, especially for the wide fan-in dynamic gates. These wide fan-in gates are one of the most important building blocks in the critical path of modern microprocessors. Their applications are related to the read path of register files, L1 caches, match lines of the TCAMs, flash memories, tag comparators, PLAs and wide MUX and De-MUX [3,4].

Moreover, energy-efficient design has been recently became an important concern especially for the portable devices as it directly affects battery life. Therefore, to achieve significant reduction in the power consumption, it is necessary to decrease all components that affect power dissipation. It is better to determine those components that have the greatest effect on the power consumption in microprocessors and embedded systems in new technology generations. As we know, power consumption of a logic gate is given by [5]:

$$P_{avg/gate} = P_{switching} + P_{short-circuit} + P_{leakage} \quad (1)$$

where, $P_{switching}$ presents the power consumed due to the charging and discharging of the circuit capacitances, $P_{short\text{-}circuit}$ is the power dissipated due to the short circuit current through V_{DD} and ground during output transitions and $P_{leakage}$ is the power consumed due to the leakage current.

The first term in (1), i.e. $P_{switching}$ is given by [5]:

$$P_{switching} = \alpha_{0\to1} C_L V_{DD} V_{swing} f \quad (2)$$

where $\alpha_{0\to1}$, called switching activity, is the probability of an output low to high transition in each clock cycle, C_L presents the load capacitance, f is the maximum possible event rate of the inputs (usually the clock rate) and V_{swing} is the maximum output voltage swing of a logic gate.

Contribution of the leakage power in the total power consumption is dramatically increased with technology down scaling and increment of temperature. This condition results in a reduction of noise immunity and robustness. Thus, it is very vital to reduce the leakage power of dynamic logic gates.

The major factor of the leakage is subthreshold current which is given by [5]:

$$I_{sub\_th} = I_0\left(1 - e^{\frac{-V_{DS}}{V_t}}\right) e^{\left(\frac{V_{GS} - V_{TH} + \eta V_{DS}}{n V_t}\right)} \quad (3)$$

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in which,

$$I_0 = \mu_0 C_{OX} \frac{W}{L}(n-1)V_t^2 \quad (4)$$

and, V_{GS} is the transistor gate–source voltage, V_{DS} is the transistor drain to source voltage, V_{TH} is the threshold voltage, $V_t = kT/q$ is the thermal voltage, η is the DIBL coefficient, n is the subthreshold swing coefficient of the transistor, μ_0 is the zero bias mobility, C_{ox} is gate oxide capacitance, W and L are the width and length of the transistor, respectively.

This paper presents a new voltage-comparison-based domino (VCD) circuit for wide fan-in applications in ultra deep submicron technologies. In the proposed circuit technique, the main goal is improving noise immunity and decreasing power consumption without significant speed degradation.

In the proposed circuit, a sense amplifier (SA) is employed to use the voltages across the pull down network (PDN) for determining the output state.

The rest of the paper is organized as follows: after the literature review in Section 2, the proposed dynamic technique is described in Section 3. A performance comparison of the proposed circuits and that of conventional circuits is performed in Section 4. Section 5 concludes the results.

2. Literature review

The conventional standard domino circuits proposed in [6] is shown in Fig. 1. The footed standard domino (FSD) circuit and the footless standard domino (SFLD) circuit are shown in Fig. 1(a) and (b), respectively.

In the evaluation phase of the domino logic, the major concern is the unavoidable leakage currents through the pull down network (PDN), even all the inputs are at the low logic level. This leakage current is due to the band-to-band-tunneling (BTBT) current, gate tunneling current and the subthreshold current. Moreover, voltage of the dynamic nodes is degraded to zero because of the charge sharing in the PDN and results in insufficient noise immunity.

In the standard domino circuit, a PMOS keeper transistor is utilized to inhibit any undesirable discharge of the dynamic node caused by the leakage currents and charge sharing of the pull down network during the evaluation phase. In this way the robustness of the circuit is improved. Although the strong keeper improves the robustness of the dynamic nodes, but there is a speed degradation and power dissipation due to the contention of the pull down network and keeper. Thus, the performance of domino gates is affected by both subthreshold leakage current and noise sources [7]. As a result, there exists a trade-off between delay and noise immunity in the standard domino gates. To provide a way performs this trade-off, the keeper ratio K is defined as the ratio of the current drivability of the keeper transistor to that of the PDN transistor:

$$K = \frac{\mu_p \left(\frac{W}{L}\right)_{Keeper-transistor}}{\mu_n \left(\frac{W}{L}\right)_{Evaluation-network}} \quad (5)$$

where, W and L denote the transistor size, and μ_n and μ_p are the electron and hole mobility, respectively. As the keeper ratio increases by keeper upsizing, noise immunity improves; however, power consumption and evaluation delay increase. These problems are more critical in wide fan-in dynamic gates due to the large number of NMOS transistors connected to the dynamic node. So keeper upsizing approach is less effective in new generations of CMOS technology.

Several circuit techniques have been proposed in the literature to address these issues. These circuit techniques can be mainly classified in two groups. Circuit techniques in the first group modify the controlling circuit of the keeper [8–32]. On the other hand, designs in the second group, including the proposed designs, modify the circuit topology of the footer transistor or reengineer the evaluation network [33–45].

Conditional Keeper Domino (CKD) technique [12] is an effective solution that uses two keeper transistors, as shown in Fig. 2. In this circuit technique, a weak keeper is employed to hold the state of the

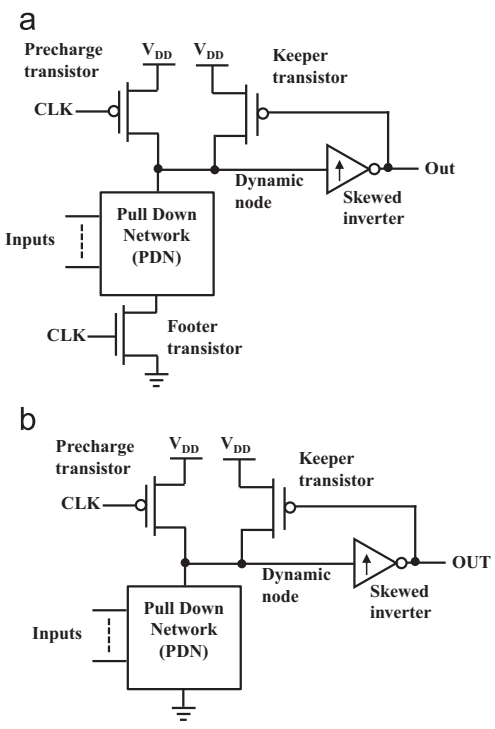

Fig. 1. Conventional domino gates, (a) with footer transistor and (b) without footer transistor.

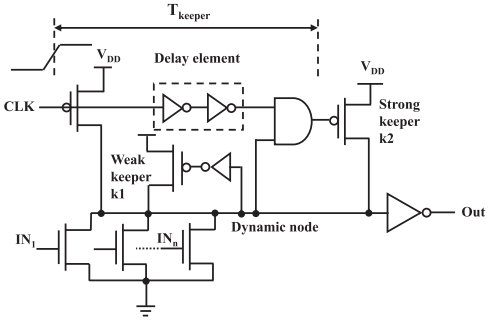

Fig. 2. A wide fan-in conditional keeper domino [12].

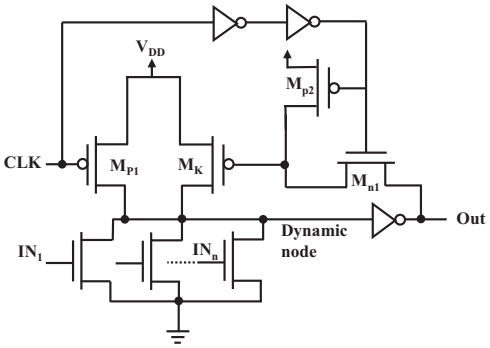

Fig. 3. HS domino logic circuit [13].