INTEGRATION, the VLSI journal 51 (2015) 149–157

Contents lists available at ScienceDirect

INTEGRATION, the VLSI journal

journal homepage: www.elsevier.com/locate/vlsi

A statistics-based digital background calibration technique for pipelined ADCs

Hamidreza Mafi [a,*], Reza Mohammadi [b], Hossein Shamsi [b]

[a] Young Researchers and Elite Club, Qazvin Branch, Islamic Azad University, Qazvin, Iran
[b] Electrical Engineering Department, K.N. Toosi University of Technology (KNTU), Tehran, Iran

ARTICLE INFO

Article history:
Received 3 September 2014
Received in revised form
23 May 2015
Accepted 26 July 2015
Available online 3 August 2015

Keywords:
Adaptive systems
Analog-to-digital conversion
Calibration
Linearization techniques

ABSTRACT

This paper introduces a digital background calibration technique for pipelined analog-to-digital converters (ADCs). The proposed method continuously measures and digitally corrects conversion errors resulting from residue amplifier gain error and nonlinearity. It is based on modulation of the residue voltage using a pseudorandom-noise sequence (PN). A least-mean-squares (LMS) algorithm is utilized to correct conversion errors arising from the residue amplifier non-idealities. Besides, a new statistics-based digitized residue distance estimation (DRDE) algorithm is proposed that allows the LMS algorithm to operate in the background without interrupting the normal operation of the ADC. The DRDE method extracts the residue amplifier non-idealities by evaluating the digitized residue voltage probability density function (PDF). Behavioral simulation results verify the usefulness of the proposed calibration technique and show that the signal-to-noise-and-distortion-ratio (SNDR) is improved from 43 to 71.9 dB, in a 12-bit pipelined ADC.

1. Introduction

Pipelined analog-to-digital converters (ADCs) are widely used in high-speed and high-resolution applications [1–6]. Although deep-submicron technologies are used to design high-speed pipelined ADCs, reduction in power supply and intrinsic gain of transistors makes the design of high-accuracy residue amplifiers strongly difficult [3,5]. Unfortunately, pipelined ADCs are sensitive to the residue amplifiers non-idealities in their first stages [2,5]. Hence, the design of high-resolution ADCs becomes more and more difficult [2]. Because of low-power digital signal processing availability in modern CMOS technologies, digital compensation of analog circuit imperfections is becoming popular [9]. In order to correct conversion errors, different digital calibration techniques for pipelined ADCs have been proposed, such as [1–18].

Digital calibration methods are divided into foreground and background categories [8]. Foreground calibration techniques identify and correct non-idealities at the startup of the ADC. Therefore, environmental changes after calibration such as temperature, supply voltage drift and device aging can result in new conversion error. In contrast, digital background techniques can continuously track and correct the errors resulted from temperature variations, supply voltage drift, and device aging at the normal operation of the ADC [8–10].

Digital background calibration techniques often exploit calibration signals such as *pseudorandom-noise sequence* (PN) to determine and correct the ADC conversion errors [1–5]. In practice, residue amplifier nonlinearities must be considered in high-resolution applications, whereas the majority of digital background calibration techniques only correct the residue amplifier gain error. It is worth mentioning that there are five background calibration techniques which can identify and correct residue amplifier nonlinearity using pseudorandom-noise sequences [1–5]. Among these techniques, the proposed technique in [1] is statistics-based and it can correct *gain*, *second*-, and *third*-order error terms. But, it has two main drawbacks: first, the *distance* between the two residue curves at the two states is estimated based on *statistics-counting* which needs an array of counters. The number of counters is exponentially proportional to the resolution of ADC [3]. Using a large number of counters in high-resolution ADCs increases complexity and power consumption. Moreover, because of the allocated time to the counters, the convergence time of this method is very long.

This paper introduces a new digital background calibration technique for pipelined ADCs. In this technique, a novel statistics-based *digitized residue distance estimation* (*DRDE*) is proposed to extract residue amplifier non-idealities without the need for a large number of counters. Besides, a *least-mean-squares* (LMS) algorithm is exploited to digitally correct conversion errors caused by residue amplifier nonlinearities. In addition, the convergence time of the proposed scheme is approximately 5 times faster than that of [1]. The rest of the paper is organized as follows: Section 2

* Corresponding author.
E-mail addresses: h.mafi.qiau@gmail.com (H. Mafi), shamsi@eetd.kntu.ac.ir (H. Shamsi).

http://dx.doi.org/10.1016/j.vlsi.2015.07.014
0167-9260/

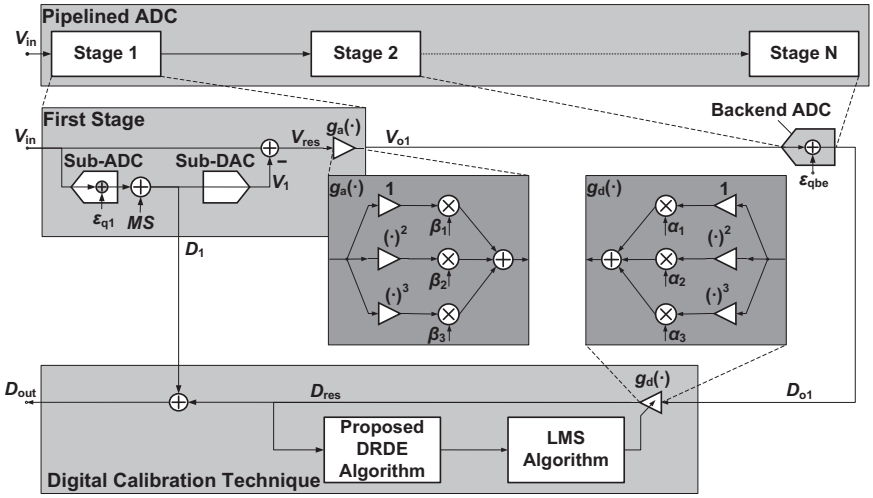

Fig. 1. Pipelined ADC architecture with the digital calibration technique.

reviews the structure of pipelined ADCs and digital error correction. Section 3 introduces the proposed digital background calibration technique. Section 4 provides the simulation results and discussions, and finally Section 5 concludes the paper.

2. Pipelined ADCs architecture and digital error correction

Fig. 1 shows the architecture of a pipelined ADC. For simplicity, the paper focuses on the calibration of the first stage and all the remaining stages are considered to be ideal and modeled by a backend ADC as in [9]. Furthermore, all signals are normalized to one and assumed as unit-less quantities. As shown in Fig. 1, each stage consists of a sub-DAC, a sub-ADC, and a residue amplifier. Since the purpose of the proposed technique is to correct the residue amplifier nonlinearity; therefore, both the sub-ADC and the sub-DAC at the first stage are also considered to be ideal. From Fig. 1, the digital output of the sub-ADC is given by

$$D_{sub1} = V_{in} + \varepsilon_{q1} \tag{1}$$

where V_{in} and ε_{q1} denote the sampled input voltage and the quantization error of the sub-ADC, respectively. If the sub-ADC has a resolution of B bits, *then* the sub-ADC has 2^B output levels with the step-size $\Delta = 2/2^B$. In addition, the sub-ADC quantization error, ε_{q1}, is restricted to the range $[-\Delta/2, +\Delta/2]$. As illustrated in Fig. 1, an additive two-level *modulation signal* (*MS*) is applied to the output of the sub-ADC in order to extract and correct the residue amplifier non-idealities [1–3,5]. The modulation signal is generated as follows:

$$\begin{aligned} &MS = \tfrac{\Delta}{2} PN, \\ &PN \in \{-1, 1\} \end{aligned} \tag{2}$$

where *PN* denotes a *two-level zero-mean* pseudorandom-noise sequence. Moreover, *PN* is independent from the sub-ADC quantization error. It follows from Fig. 1 and Eq. (1) that the digital output of the first stage is given by

$$D_1 = V_{in} + \varepsilon_{q1} + MS. \tag{3}$$

The ideal task of the sub-DAC is to convert D_1 to its analog representation, V_1. Hence, as depicted in Fig. 1, the first stage *residue voltage* is given by

$$V_{res} = V_{in} - V_1. \tag{4}$$

From (3) and (4), the residue voltage is represented by

$$V_{res} = -\varepsilon_{q1} - MS. \tag{5}$$

It follows from Fig. 1 and Eq. (5) that the residue voltage is the sum of the sub-ADC quantization error and the modulation signal. Since the modulation signal is independent from ε_{q1}, hence, it is clear to prove that the residue voltage is restricted to the range $[-\Delta, +\Delta]$. The residue amplifier, g_a, amplifies V_{res} to generate the first stage output voltage $V_{o1} = g_a(V_{res})$. Ideally, the nominal gain of the residue amplifier is chosen such that the residue voltage is scaled to the interval $[-1, 1]$ [3]. Consequently, the residue amplifier gain must be identical to $1/\Delta$. Furthermore, to design a B-bit stage with the injection of the modulation signal, a $(B+1)$-bit sub-ADC with step-size $\Delta = 1/2^B$ and a residue amplifier with a nominal gain of 2^B $(=1/\Delta)$ must be employed [1–3]. It is worth mentioning that, in a conventional B-bit stage (i.e., without the addition of the modulation signal), a B-bit sub-ADC and a residue amplifier with a nominal gain of 2^B are used because the residue voltage range needs to be scaled from the range $[-\Delta/2, +\Delta/2]$ to the interval $[-1, 1]$ [1–3]. In summary, in order to accommodate the injection of the modulation signal, the sub-ADC resolution needs to be increased by 1 bit in almost all background calibration schemes. Besides, using this mechanism, the maximum magnitude of the residue voltage with the injection of the modulation signal does not increase compared to the conventional pipelined stage [9].

In modern CMOS technologies, the residue amplifier, g_a, is often modeled as a *memory-less weakly-nonlinear* function [2,3]. Therefore, the input–output characteristic function of a well-designed residue amplifier can be approximated accurately by a *third-order polynomial* as follows:

$$V_{o1} = g_a(V_{res}) \approx \beta_1 V_{res} + \beta_2 {V_{res}}^2 + \beta_3 {V_{res}}^3 \tag{6}$$

where β_1 represents the residue amplifier *gain*, and β_2 and β_3 denote the residue amplifier *second* and *third*-order nonlinear errors [1,4], respectively. The ideal backend ADC digitizes the output voltage V_{o1} into D_{o1} as follows:

$$D_{o1} = V_{o1} + \varepsilon_{qbe} \tag{7}$$

where ε_{qbe} denotes the backend ADC quantization error.

The digitized output voltage, D_{o1}, is applied to the *digital error correction block*, g_d. The goal of g_d is to remove the errors of D_{o1} due to the nonlinear residue amplifier, g_a. Therefore, the digital error correction block must be the inverse function of the residue amplifier [4,9]. In practice, the inverse function, g_a^{-1}, can also be approximated by a third-order polynomial. Consequently, D_{o1} is