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Fast and scalable parallel layout decomposition in double patterning lithography ☆

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ABSTRACT

For 32/22 nm technology nodes and below, double patterning (DP) lithography has become the most promising interim solutions due to the delay in the deployment of next generation lithography (e.g., EUV). DP requires the partitioning of the layout patterns into two different masks, a procedure called *layout decomposition*. Layout decomposition is a key computational step that is necessary for double patterning technology. Existing works on layout decomposition are all single-threaded, which is not scalable in runtime and/or memory for large industrial layouts. This paper presents the first window-based parallel layout decomposition methods for improving both runtime and memory consumption. Experimental results are promising and show the presented parallel layout decomposition methods obtain upto 21 × speedup in runtime and upto 7.5 × reduction in peak memory consumption with acceptable solution quality.

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1. Introduction

As VLSI technology nodes proceed beyond 32 nm/22 nm and below, the next generation lithography (NGL), such as Extreme Ultraviolet (EUV), is still facing both technology and cost challenges for mass production. As a result, double patterning (DP) lithography technology has become the most feasible interim solution [1]. DP requires that the dense circuit patterns be partitioned into two separate exposures, which decreases the pattern densities in each exposure and thus improves resolution and depth of focus (DOF). DP layout decomposition must satisfy the following requirement: two patterns must be assigned opposite colors (corresponding to different mask exposures) if their spacing is less than the *minimum coloring spacing* [2].

There has been a large body of work on single-threaded DP layout decomposition. Kahng et al. proposed different DP layout decomposition and coloring approaches based on integer linear programming (ILP) and graph bipartization algorithms [2–4]. Yuan et al. developed an ILP algorithm to minimize the number of conflicts and stitches simultaneously based on a grid layout model [5]. Xu and Chu proposed a graph-based method for reducing the problem size and thus speeding up the ILP solution [6]. A simultaneous layout decomposition and migration method for standard cells based on ILP formulation [7] was proposed by Hsu et al. Yang et al. presented a heuristic minimum-cut-based graph bipartization algorithm for DP layout decomposition considering both balanced density and timing optimization [8]. A graph-matching based method on a constructed face graph was proposed by Xu and Chu [9]. Luk and Huang used an SPQR-Tree data structure to reduce the layout decomposition problem size for runtime speedup without degrading the solution quality [10]. Ban et al. presented a layout decomposition framework for spacer-type double patterning [11]. There were also works considering the DP requirements during both the routing stage [12–14] and post-routing optimization stage (e.g., wire spreading, layer assignment, etc.) [15–17].

All the above works present single-threaded algorithms for optimizing the DP objectives, such as the number of coloring conflicts, stitches, etc. With the rapid deployment of multi-core CPUs and commodity computational clusters, parallel computation is becoming necessary to achieve the great performance and scalability [18–20]. Although the graph partitioning methods in [6,10] can be easily extended for parallel processing, they require that the whole layout be loaded in and the whole corresponding graph be constructed, which consume huge memory for large layouts. This paper presents *window-based* scalable parallel DP layout decomposition methods, which avoid the construction of the whole graph to save memory consumption. The presented methods are generic in the sense that the graph partitioning methods in [6,10] can still be used in each window for further speedup. Major contributions of the paper are as follows.

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- We present and compare two parallel layout decomposition approaches, including a maximum independent set-based parallel (MISP) method and a stochastic optimization-based parallel (SOP) method, which make the existing single-threaded layout decomposition algorithms more practical and applicable for large industrial layouts.
- The MISP method partitions the original layout decomposition problem into sets of sub-problems, where the sets are processed in sequential manner and sub-problems in each set are processed in parallel. The MISP method obtains notable improvements in both runtime and memory, with a little degraded solution quality. The SOP method can further improve the solution quality using the Cross Entropy method [21] with increased runtime. The two parallel methods can be selected in real applications depending on the available servers in the computational cluster.
- The two parallel methods use an overlapping window-based scheme, which avoids large memory consumption for constructing the whole graph of large layouts. The window-based scheme can be used in conjunction with any specific single-threaded layout decomposition algorithm. Besides, the presented parallel methods do not make any assumptions about the machine architecture and hence are very generic.

The rest of the paper is organized as follows. An overview of the double patterning lithography and the associated layout decomposition problem is given in Section 2. Section 3 presents the flows of the parallel methods for layout decomposition. An overview of the window construction process is given in Section 4. Sections 5 and 6 present the details of the MISP and SOP parallel flows, respectively. Experimental results are presented in Section 7. Section 8 concludes the paper with future research directions.

2. Preliminaries

2.1. Double patterning technology

There are basically two types of multiple exposure techniques with different lithography patterning steps, i.e., pitch splitting (PS) and spacer patterning (SP) [1]. PS includes double patterning (DP) and double exposure (DE). For patterning a single device layer, the DP process consists of two separate and sequential lithography/etch steps (i.e., litho etch litho etch, LELE). By contrast, the DE process includes two lithographic exposures followed by one etch step. Though one etch step is saved in DE with reduced manufacturing cost, the images formed by the two exposure steps may interact with each other, which results in degraded resolution [22]. Different from DP and DE, the SP process uses only one exposure step, an additional thin film deposition and two etch steps to define a single device layer. The allowable patterns on the device layer is restricted in SP. We focus on the DP process in this paper, which can also be extended for the DE process.

Double patterning technology requires layout patterns be split into two separate mask exposures, such that the decreased pattern density on each mask can improve resolution and DOF. Typically, a manufacturing process-dependent *minimum coloring spacing t* is used for the pattern splitting [2]. Where there are two layout patterns with distance less than t, they need to be assigned to different masks.

Fig. 1 gives an example illustrating how the DP process improves the resolution. In the figure, the distances between the adjacent rectangular layout patterns are d_1. Assume $d_1 < t$. Then the layout patterns are assigned to different masks as denoted with different colors (i.e., gray and blue). This ensures that for each separate exposure the minimum distance between adjacent patterns is increased, i.e., $d_2 = d_3 > t > d_1$, thereby improving the resolution and DOF.

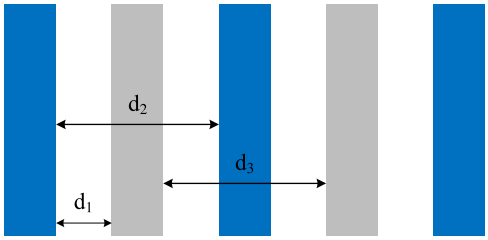

Fig. 1. Example of resolution improvement using the DP process. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

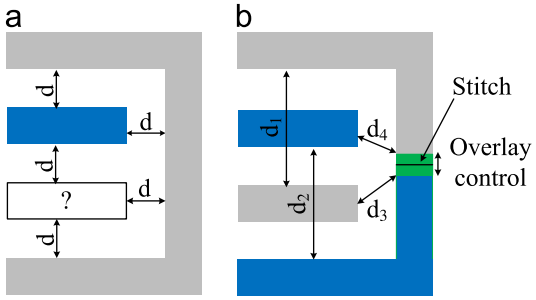

Fig. 2. Stitches further improve resolution. (For interpretation of the references to color in this figure caption, the reader is referred to the web version of this article.)

2.2. DP layout decomposition and coloring problem

For a given t, certain layout configurations cannot be successfully assigned to either mask, i.e. assigned a gray or blue color, without violating the minimum coloring spacing t. This is called a *coloring conflict*. Fig. 2 gives an example. In Fig. 2(a), assume $d < t$. Then the gray pattern with a question mark cannot be assigned either a gray or blue color without violating the minimum coloring spacing. Fig. 2 (b) shows a feasible coloring solution where the U-shape pattern is split into two parts and a *stitch* is introduced. At each stitch, the line-end is extended to guarantee the overlay control between the two mask exposures [2]. From Fig. 2(b), we have $d_1 = d_2 > d_3 = d_4 > d$. Assume $d < t < d_3$. Then, the coloring conflict can be solved by splitting the given pattern with a stitch. Pattern splitting with introduced stitches is a major factor distinguishing between the strong alternating phase-shift mask (AltPSM) and the DP layout decomposition problems [23].

Formally, the DP layout decomposition and coloring problem is as follows: *Given a layout and a distance t, find a pattern splitting and color assignment solution for all the layout patterns such that the total cost is minimized, subject to the constraint that non-overlapping shapes within distance t be assigned different colors.*

The total cost can incorporate different objectives, such as minimizing the coloring conflicts,[1] minimizing the number of stitches for better overlay robustness, and other possible timing and yield related objectives.

3. Overview of the parallel layout decomposition flows

3.1. Maximum independent set-based parallel flow

Fig. 3 shows the overall parallel layout decomposition flow based on the MISP approach.

[1] Even with pattern splitting, there may still be coloring conflicts due to specific pattern combinations or sub-optimality of the color assignment algorithm.

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