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Nano-CMOS thermal sensor design optimization for efficient temperature measurement

Oghenekarho Okobiah [a,b], Saraju P. Mohanty [a,b,*], Elias Kougianos [a,c]

[a] NanoSystem Design Laboratory (NSDL), University of North Texas, Denton, TX 76207, USA
[b] Department of Computer Science and Engineering, University of North Texas, USA
[c] Department of Engineering Technology, University of North Texas, USA

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ABSTRACT

We present a novel and efficient thermal sensor design methodology. The growing demand for power management on VLSI systems drives the need for accurate thermal sensors. Conventional design techniques for on-chip thermal sensors in nanometer technologies consume expensive design iterations and result in increased power consumption and area overhead. Power-efficient, high-sensitivity thermal sensors are important for reducing the thermal stress on the systems or circuits which are being monitored. The proposed design flow methodology, which incorporates a stochastic gradient descent (SGD) algorithm, optimizes the power consumption (including leakage) of IC subsystems. An illustration of the proposed design methodology is presented using a ring oscillator (RO) based on-chip thermal sensor which was designed using 45 nm CMOS technology. The RO based thermal sensor has a resolution of 0.097 °C/bit. Experimental tests and analysis of the design methodology on a full layout-accurate parasitic netlist of the RO demonstrate the applicability of our methodology towards optimization of the power consumption with temperature resolution as a design constraint. A reduction of power consumption by 52% with a final area of 1389.1 μm^2 is obtained.

1. Introduction

The increasing complexity and power consumption of Systems-on-Chip (SoCs) continues to grow as technology shrinks due to scaling. The density of modern integrated chips (ICs) and SoCs results in very high on-chip power densities. The increase in power consumption and power density is a critical issue, directly affecting the thermal stability of SoCs. To mitigate these issues, various thermal management schemes have been explored for efficient control of power density of ICs. Thermal sensors are typically used for controlling the power consumption and to increase the reliability of SoCs. Thermal sensors are needed for effective thermal management which helps to reduce power consumption and increase performance. Approximately 50% of reliability issues are attributed to thermal related causes [1]. To monitor and effectively control the thermal properties of integrated devices, the accuracy of thermal measurements must be ensured. Hence, the importance of on-chip thermal sensors. They are one of the most common methods of measuring the thermal characteristics of ICs [2] and depending on the application, an IC may contain multiple such sensors. The placement of on-chip thermal sensors on an example motherboard is shown in Fig. 1.

The design of thermal sensors for different applications has been widely researched and reported [3–8]. Such designs using CMOS technology have been reviewed in [8,7] and extended its applications to on-chip sensors in [4,5]. Thermal sensors based on CMOS technology utilize the temperature dependent characteristics of MOS transistors for sensing the temperature of the circuit [5]. Oscillator based designs are one of the most common techniques of CMOS based thermal sensors, where the oscillating frequency depends on temperature and is converted to temperature readings. The use of thermal sensors on chips, however, contributes to some problems. Poorly designed sensors can decrease the performance by adding an area overhead and increasing the overall power consumption. In [6], the power consumption of the on-chip thermal sensor significantly increases the overall power consumption. In effect, integrated thermal sensors for SoCs must also be low-power and cost-effective area wise. In addition, the sensors must accurately measure the temperature of the chip which puts more constraints on the low-power specification. Hence, the design of thermal sensors themselves has also become an integral part of reliability designs. Recent research works [4,5] have proposed solutions for efficient

* Corresponding author at: Department of Computer Science and Engineering, University of North Texas, USA. Tel.: +1 9405653276.
E-mail addresses: oo0032@unt.edu (O. Okobiah), saraju.mohanty@unt.edu, sarajupmohanty@gmail.com (S.P. Mohanty), elias.kougianos@unt.edu (E. Kougianos).
URL: http://nsdl.cse.unt.edu (O. Okobiah).

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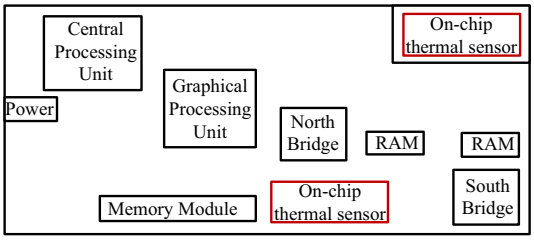

Fig. 1. Thermal sensor locations on a motherboard.

on-chip thermal sensors which are low-power and do not significantly impact the circuit intended for sensing. In designing for low power consumption, other factors such as thermal sensitivity are often traded for optimization. Thermal sensors for on-chip use must be robustly designed to efficiently control the problems of power density without increasing the overall power consumption or incurring more cost from area overhead or degradation of the thermal sensitivity. In the optimization of design for performance objectives, various search algorithms are used for efficient design space exploration. Common search algorithms that have been implemented for the optimization of nanoCMOS circuits include genetic algorithms, swarm intelligence algorithms, geometric programming, simulated annealing, tabu search and gradient search algorithms [9–12].

In order to mitigate the problems of on-chip temperature measurement, this paper proposes a design optimization flow methodology for the design of efficient on-chip thermal sensors. The proposed methodology incorporates a stochastic gradient descent based (SGD) algorithm. The use of optimization algorithms to increase the speed of explorative search designs has also been widely reported. The use of an SGD algorithm improves the design process by reducing the design space exploration time for optimization. The modified SGD algorithm also eliminates the problem of local optima. The design flow is presented using a 45 nm thermal sensor as case study circuit. In illustrating the effectiveness of the design flow, the power consumption of the thermal sensor is reduced using the accuracy of the temperature measurements as a constraint.

The rest of this paper is organized as follows. The novel contributions of this paper are presented in Section 2. A brief review of selected related research is presented in Section 3. In Section 4, a description of the baseline design of a thermal sensor circuit using 45 nm CMOS technology is presented. The proposed design optimization flow methodology is presented in Section 5. The experimental setup, results and analysis are presented in Section 6. In Section 7, conclusions and future research directions are discussed.

2. Novel contributions of this paper

This paper presents a novel design flow methodology incorporating the use of a Stochastic Gradient Design (SGD) based algorithm for the efficient design optimization of analog circuits. An on-chip thermal sensor using a 45 nm technology is used as an illustrative case study. The schematic and physical designs of the sensor are presented. The sensor is based on a ring oscillator (RO) architecture that uses a binary counter and registers for accurate temperature measurement. The SGD based algorithm also presented here is applied on nano-CMOS circuit designs for the first time. The standard SGD algorithm has been modified to restart at random points in order to mitigate the issue of local optima of the traditional SGD algorithm. A further analysis of the impact of process variation on the power consumption performance of the thermal sensor is also discussed.

A *summary of the contributions* of the current paper are as follows:

1. A robust design flow is proposed to design and characterize nano-CMOS based thermal sensors.
2. A design optimization methodology is presented for fast design exploration of thermal sensors.
3. A modified Stochastic Gradient Descent (SGD) algorithm is presented for thermal sensor optimization.
4. A 45 nm RO based thermal based sensor is designed at the layout level and optimized.
5. A statistical analysis of the impact of process variation of power consumption was performed on the thermal sensor.

3. Related research on temperature sensors

The design of on-chip thermal sensors, including design for accurate temperature estimation and robust performance, has been well researched [4,5,13,7,3,14]. In [5], a class of thermal sensors based on Differential Ring Oscillators (DRO) is introduced. An implementation using a current starved inverter topology utilizes the sensitivity of the oscillating frequency to temperature for thermal sensing. In [6], a low power thermal sensor has been proposed. It employs an oscillator based on an RS register structure. The output frequency of the oscillator is Proportional to Absolute Temperature (PTAT) and is thus used with a constant pulse generator and a bias calibrator. In [13], another approach is taken to compensate for the effect of noise, process variations and V_{DD} fluctuations on the thermal sensor. A statistical methodology is proposed for estimating the actual temperature reading of the sensor. The temperature is modeled as a variable associated with a probability density function (PDF) that is dependent on the noise, process variations and V_{DD} fluctuations. In [15,16], a PTAT current source is proposed. The circuit uses the ratio between the drain currents of two current source transistors operating in the subthreshold region which is PTAT for thermal sensing. The source transistors are fed by a reference current which is independent of ambient temperature and the output of the PTAT generator is converted to a corresponding temperature reading with an A/D circuit [16]. In an effort to reduce the effect of process variation and noise on thermal sensors, similar circuits have been proposed in [17]. In [3], a technique implementing inductors and variable capacitors is proposed for thermal sensing of high temperature environments. The temperature reading is telemetrically placed outside of the circuit to isolate it from the high temperatures on the circuit.

A recent design has been proposed in [14] that implements a miniaturized CMOS based thermal probe that significantly reduces the size of comparable sensors allowing it to be easily placed near hot spots for localized real-time temperature mapping. The thermal sensor design presented in this paper is also oscillator based and is motivated by the design presented in [4]. The sensor used is implemented using the conventional ring oscillator topology in contrast to the current starved topology. The thermal sensor is also not operated in the subthreshold region which leads to a decrease in frequency with increasing temperature. The frequency divider and multiplexer are eliminated in our design.

4. Thermal sensor design for on-chip temperature measurement

The 45 nm thermal sensor used as an illustrative application of the proposed design flow methodology is presented in this