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Low power wide gates for modern power efficient processors

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ABSTRACT

In this paper, a low power register file and tag comparator is proposed which has lower leakage and higher noise immunity without dramatic speed degradation due to the wide fan-in gates. Simulation of register files and tag comparators designed is done using low-V_{th} 90 nm CMOS process technology model in all process corners. The results demonstrate 20% power reduction and 2× noise-immunity improvement in the implemented register file using the proposed circuit at the same delay compared to the standard domino circuits. On the other hand, simulation of tag comparators implemented using the other proposed circuit shows 41%, 22% and 7.5% reduction in power, delay and area, respectively compared to the standard footless domino at the same robustness condition. Moreover, the register file and the tag comparator designed with the proposed circuits respectively show 2.48 and 3 times improvement in the defined figure of merit compared to the counterpart circuits designed with the conventional domino circuit. Thus, the proposed are power efficient and suitable approaches for embedded processors with multi-ported register file and fully-associative caches with large number of tag comparators.

1. Introduction

Dynamic logic circuits such as domino are widely used in many applications to achieve the high performance that cannot be achieved with static logic styles [1]. However, the main drawback of dynamic logic families is that they are more sensitive to noise. On the other hand, as the technology scales down, the supply voltage is reduced for low power, and the threshold voltage (V_{th}) is also scaled down to achieve high performances. However, reducing the threshold voltage exponentially increases the subthreshold leakage current. Therefore, a reduction of leakage current and an improvement noise immunity are of major concern in robust and high performance designs in recent technology generations, especially for wide fan-in dynamic gates [2] which are typically employed in the read path of register files, L1 caches, match lines of TCAMs, flash memories, tag comparators, PLAs and wide MUX and De-MUX. Among these devices, the register files and tag comparators are more important in modern microprocessors since they are one of the most critical modules in their critical paths [3].

The Intel Pentium 4 processor architecture includes two register files in the data path which are the integer register file, and the floating point register file, denoted by Integer RF and FP RF in Fig. 1, respectively [4]. Since data are read from or written to these register files in each instruction execution, fast register file circuits are critical to achieve high-performance in microprocessors [3]. A register file consists of an array of SRAM-based registers, a write port, and a read port as shown in Fig. 2.

These ports are mainly realized by utilizing multiplexer and de-multiplexer circuits which are typically implemented by OR and NOT gates. In a register file with 2^n registers, n-bit address lines, $(n+1)$-input intermediate OR gates and a $2n$-input output OR gate is needed [5]. Therefore, wide fan-in OR gates are one of the most important building blocks for the implementation of high-performance modules. However, in wide fan-in dynamic gates especially wide fan-in OR gates, robustness and performance significantly degrade with increasing leakage current. As a result, it is difficult to obtain satisfactory robustness-performance tradeoff.

To achieve dramatic performance by exploiting instruction level parallelism and memory locality, implementation of multi-ported register files and larger caches is necessary to feed data paths of multiple functional units and to store global variables for general-purpose microprocessors and embedded systems. However, increasing the switching capacitance due to the use of more transistors and larger on-chip components causes a significant increase in energy consumption. Therefore, the power dissipation of memory structures such as caches and register files will increase significantly with new generations of process technologies.

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This paper describes a 64-word × 32-bit 2-read, 1-write ported register file designed and a tag comparator using the proposed circuit techniques for low operation in $1-V$ low-V_{th} 90-nm CMOS technology. The proposed designs employ a footer transistor in diode configuration to reduce leakage current and exploit a mirror current to compare the current of the evaluation network with its worst case leakage current to determine the output state, yielding lower contention current and higher performance.

The rest of the paper is arranged as follows: after a discussion of the sources of power dissipation and literature review in Sections 2 and 3, the proposed designs for the register files and tag comparators are described in Section 4. Section 5 will include simulation results for the proposed designs using HSPICE simulations in low-V_{th} 90 nm CMOS process technology compared with other conventional circuits. Section 6 concludes the results.

2. Sources of power dissipation

Energy efficiency becomes an important issue especially for portable computing because it directly affects battery life. Therefore, to achieve significant reduction in power consumption, it is necessary to determine those devices that have the greatest effect on the power consumption in microprocessors and embedded systems.

As we know power consumption of a logic gate is given by:

$$P_{avg/gate} = P_{switching} + P_{short-circuit} + P_{leakage} \quad (1)$$

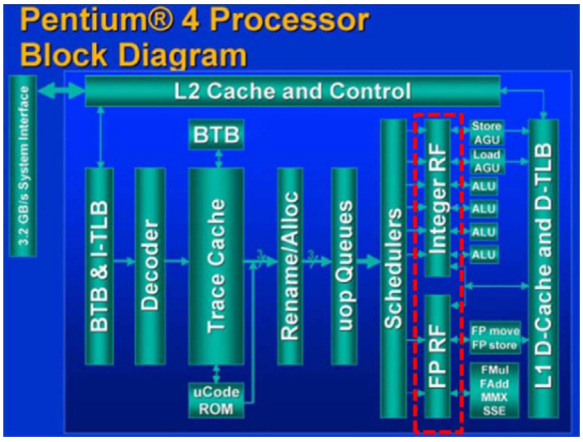

Fig. 1. Block diagram of Pentium 4 [4].

where $P_{switching}$ is the power consumed due to charging and discharging of the circuit capacitances, $P_{short-circuit}$ is the power consumed due to the short circuit between V_{DD} and ground during output transitions and $P_{leakage}$ is the power consumed due to leakage current.

The last term, i.e. $P_{leakage}$ is dramatically increased with technology down scaling and increase of temperature, resulting in a reduction of noise immunity and robustness. Thus, it is very vital to reduce the leakage power of dynamic logic gates.

Devices that have higher switching capacitance such as memories or work continuously such as clock network are main candidates for these policies. The clock tree, as obtained in [6], consumes almost 40% of the total power of the arithmetic data path and also consumes from 20% up to 45% of the overall power consumed in a dynamic system as demonstrated in [7]. For example, clock network consumes 32% of total power consumption in Alpha 21364 [8]. The long clock tree and the undesired switching activity are the major reasons for that. To eliminate the clock tree, asynchronous or self-timed designs must be used.

Memory devices which include on-chip main memory, caches, register files, instruction and load-store queues (LSQ), re-order buffer (ROB) and branch prediction tables (BPT) occupy a large area and consume significant power in current microprocessors.

Multi-ported register files consume 25% and 37.1% of the overall power in embedded processors and in a network-on-chip (NOC) platform, respectively when running average applications [9]. Since size and access time of register files are expected to increase in future microprocessors, they will likely consume more power because of continuous operation cycle. Unlike other architectural modules, register files are always clocked and the clock gating technique for power reduction is not applicable for register files. Thus, the register file becomes one of the dominant factors in power consumption of embedded processors.

Cache memories are the other device that consumes a significant amount of power. In Alpha 21364, 128 KB of on-chip cache consumes 15% of total power [10]. Other examples are on-chip caches for Strong ARM SA110 [11] and 300 MHz bipolar CPU [12] which consume 43% and 50% of the overall power. Among the caches types, highly-associative caches with content-addressable-memory (CAM) tags have the lowest miss rates because each memory location can be anywhere in a sub bank, but the majority of energy is spent in the tag check and mainly in the tag comparators. Unlike highly-associative caches, direct mapped caches generally have lowest power consumption and highest miss rate. Thus, there is a tradeoff between miss rate and power consumed for tag check.

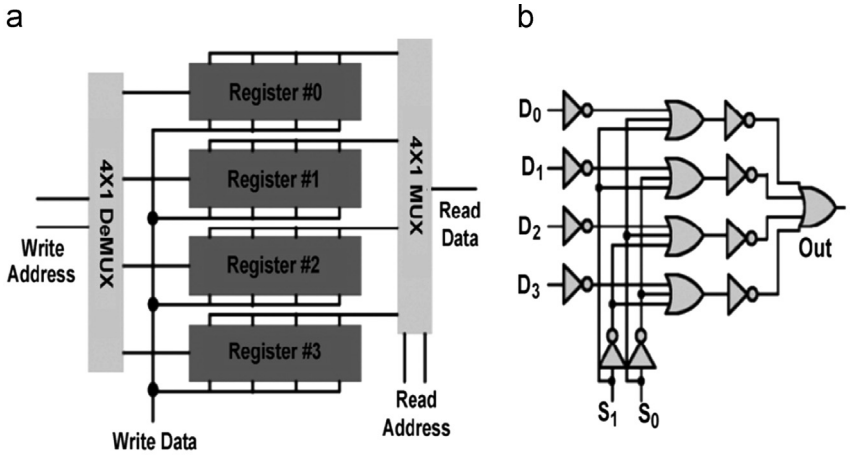

Fig. 2. (a) Simplified register file block diagram and (b) implementation of read port using 4 × 1 multiplexer [3].