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Customizing completely specified pattern set targeting dynamic and leakage power reduction during testing

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ABSTRACT

In this work, we propose a technique to reduce switching activity while keeping leakage current under control during testing by extracting don't cares from a completely specified pattern set, and using the *X* bits to convert original vectors into low power vectors by a dictionary based approach. We also investigate the possibility of reducing test set length, maintaining fault coverage, by performing a tradeoff between test set volume and power. Experiments on ISCAS89 benchmark circuits validate effectiveness of our work. We could achieve an average reduction of 84.78% in dynamic power and 6.52% in leakage power for pattern set generated by the ATPG tool Atalanta. Similar savings could also be achieved on test set generated by the commercial ATPG tool Tetramax.

1. Introduction

Automated Test Pattern Generation (ATPG) tools generally work in two phases. Initially, a random pattern generation scheme is employed, as long as the fault coverage of the generated test set continues to improve with the addition of further patterns. However, due to the presence of random pattern resistant faults, the fault coverage saturates after some time. That is, covering further faults require generation of a large number of non-detecting patterns (that do not identify any new fault). Next the ATPG tool switches over to deterministic test pattern generation for the remaining faults. At this stage, the generated patterns often contain a large number of don't care bits, that is, many of the inputs are left unspecified. The output test pattern set, at the end of random and deterministic test generation stages, is usually huge. The pattern set is then compacted, since the faults detected by a pattern discovered early in the generation process, may be covered by the test pattern(s) added later to the set. Various compaction strategies have been tried out in the literature. Test compaction algorithms, like reverse-order fault simulation [1] and double detection [2], fail for patterns with unspecified bits in them. On the other hand, dynamic compaction cannot take advantage of random test generation phase, since this is fault oriented [3]. Hence, the situation creates the opportunity to look back into the test pattern set (which is mostly completely specified, considering the compaction process) generated by an ATPG tool, and extract don't cares from it. The resulting patterns (with don't cares) can then be utilized for various purposes, such as, better compaction, lesser power and energy consumption during testing, test length vs. test energy tradeoff, etc.

The reverse process of *X*-identification locates the bits in a given pattern set that can be turned to don't cares (*X*) without affecting the fault coverage and preferably test length. The idea of *X* bit identification has been introduced in [4,5]. Authors of [6] have proposed two approaches for the same objective. The first one is a brute-force technique, where every bit of the test vector is checked to see whether changing it to *X* reduces the fault coverage or not. This technique does not work for large circuits. The second method uses a technique based on critical path tracing (CRIPT) algorithm. In this approach, the fault activation path is also considered along with the fault propagation path. Controllability cost functions [7,8] are used to justify required values through assignment to the smallest number of primary inputs. It also proposes a fanout based controllability function in addition to the recursive controllability cost function. Though fanout based cost function can give better results, it is not consistent across all the circuits. So, a weighted cost function has been introduced to select the primary inputs that should remain specified. This approach uses an event driven procedure to select the primary output to which the fault propagates to, whereas the brute force method implicitly selects the output to which the fault propagates according to the order in which the test vectors are considered.

Our work is centered around identifying don't cares and using them to reduce power consumption during testing. In our approach, we follow similar implication and justification procedures as in [5]

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for fault effect propagation path. However, we proceed further to identify the *X* bits in the fault activation path as well, without sacrificing fault coverage. The identified *X* bits are next judiciously filled to reduce both dynamic and leakage power consumption. With the shrinking of feature size and increased device density, power consumption during testing has assumed high importance. Power consumption during test has been found to be much higher than during normal mode of operation [9,10]. Majority of these power reduction techniques [9,11–13] have been oriented towards reducing the switching activity in the circuit so that the dynamic power component can be kept under check. With the scaling down of physical dimensions, static power can no longer be neglected. A static estimation method that can calculate average leakage power efficiently has been given in [14,15]. However, till recently, transient leakage behavior, discussed in [16], has not been included in either dynamic or leakage power estimation. The discussion in [16] shows that the contribution of the runtime leakage power cannot be neglected for modern circuits. Thus, leakage power depends not only on the current test vector, but also on the previous vector applied to the circuit under test (CUT). In our approach, to estimate power dissipation, we consider the contribution of dynamic power along with runtime leakage power. It may be noted that the work reported in [3] presents an approach to generate test patterns rich in don't cares. However, it cannot do customization of a given pattern set.

Fig. 1 summarizes the different stages of our approach. The completely specified pattern set generated via any ATPG tool and a set of low-leakage input patterns are taken as input. The low-leakage patterns are such that, if applied at the input, the circuit will consume very small leakage power. The approach reported in [17] has been utilized to obtain the low-leakage input vectors. Starting with the completely specified pattern set, an improved don't care identification is carried out that considers both fault activation and propagation paths. It produces an incompletely specified pattern set (rich in don't cares). Since different low-leakage vectors have many of their bits similar, the strategy of aligning the incompletely specified patterns with them (and thus filling up the don't cares) generates a pattern set with reduced overall Hamming distance between the patterns. The set is then reordered to reduce power further. Next, we explore the possibility of reducing the size of the set by introducing patterns with high fault coverage into the set. The pattern set is then compacted with a new compaction algorithm. This results in a tradeoff between test length and power without compromising on fault coverage.

The salient contributions of the paper are as follows:

1. Uses an extended version of the don't care identification technique [5].
2. The identified don't cares are utilized to align each pattern with one of the low-leakage patterns for the circuit. This reduces dynamic and leakage power in both non-scan and scan circuits.
3. A Particle-Swarm Optimization (PSO) based reordering technique for the test vectors to reduce power further.

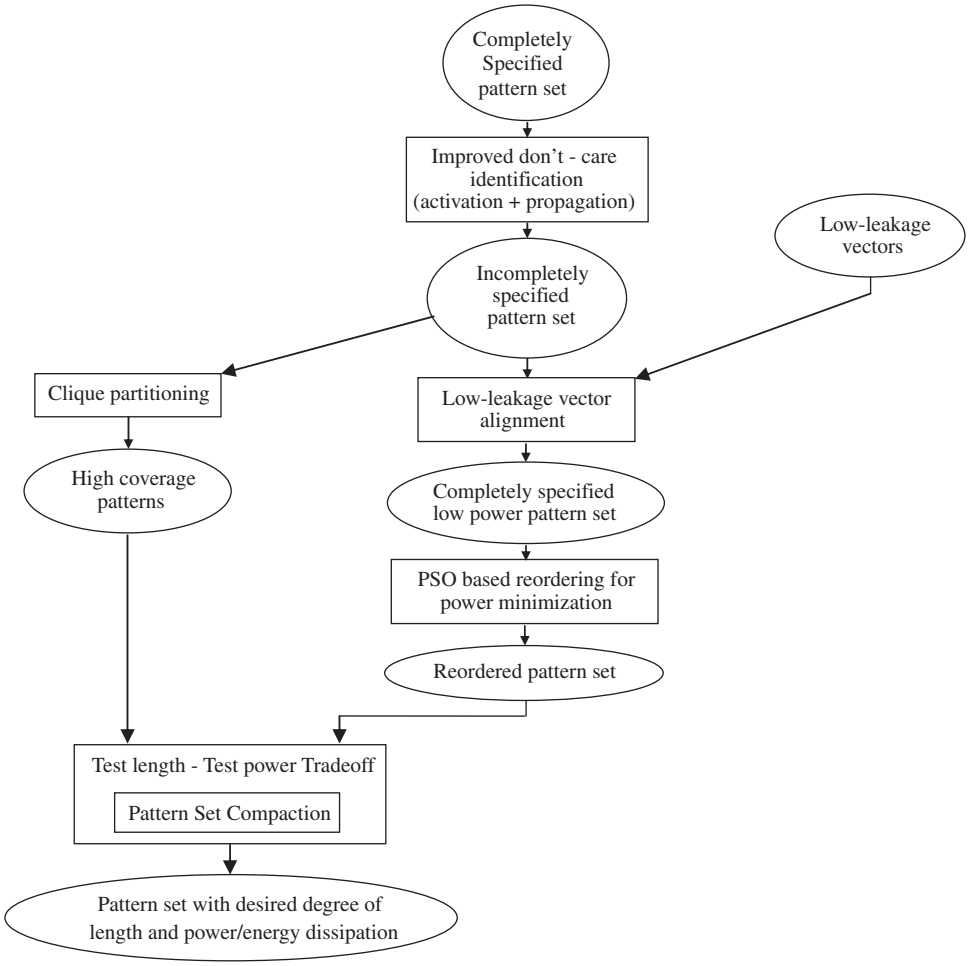

Fig. 1. Flow diagram of our approach.