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Power-efficient drive circuit for plasma display panel

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ABSTRACT

This paper proposes a power-efficient drive circuit for plasma display panels (PDPs). The proposed circuit reduces reactive power consumption by varying the inductance for energy recovery and by separating the grounds of the sustain and data drivers. Power consumption due to discharge current is reduced by using two soft-switching inductors for the pull-up switches in the bridge circuit. Power consumption for data addressing is reduced by using a dc voltage source to bias the ground for the sustain driver. The proposed circuit was tested on a 50″ full-HD single-scan PDP which had a sustain discharge gap of 80 μm; total power consumption to display the dynamic broadcasting content of IEC 62087 was ~40 W (14.5%) less than that required by the conventional drive circuit, and the EMI level for $2 < f < 9$ MHz was reduced significantly. The experimental results demonstrate that a high performance power-efficient PDP drive circuit can be built using the proposed method.

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1. Introduction

Major sources of power dissipation in the drive circuit of a plasma display panel (PDP) (Fig. 1) are ohmic loss on the sustain current path (Fig. 1, between nodes b and b'), hard-switching loss on the pull-up switches (Fig. 1, Q_{1Y} and Q_{1Z}), and switching loss on the data drive circuit. Ohmic loss on the sustain current path can be reduced by decreasing the capacitances between panel electrodes [1], by separating the ground for sustain circuit (CHGND) from the ground for data drive circuit (FGND) during the sustain period [2], or by both methods. The switching loss on the data drive circuit can be reduced by using a dc voltage bias between CHGND and FGND for the address period [3]; this bias allows use of a low-voltage data pulse.

The leading and trailing edge (Fig. 2, ER_UP and ER_DN) waveforms of sustain pulses are generated by a resonance between the energy recovery (ER) inductors (L_Y and L_Z) and the panel capacitance $C_p \equiv C_{YZ} + C_{YX}$, where C_{YZ} is capacitance between the scan electrode Y and common electrode Z, and C_{YX} is capacitance between Y and the data electrode X. The resonance current decreases as ER inductance increases, so ohmic loss on the path of sustain current can also be reduced by increasing ER inductance. An increase of ER inductance causes the sustain discharge to be unstable when the number of ON cells on the panel (picture load PL) increases, because the gas discharge starts during the ER_UP period and the initial discharge current should be supplied through the ER inductors. One approach to solve this problem is to use the current injection method [4–10] in which the initial current for ER_UP is increased by applying a voltage source to the ER inductor before ER_UP. The increased ER current helps induce the sustain discharge properly. However, the current injection method does not much improve the power efficiency for high PL because the ohmic loss on the ER current path increases to build up the initial ER current.

Another approach is to use the pull-up switches Q_{1Y} and Q_{1Z} [11]. The panel voltage V_Y increases abruptly to the sustain voltage V_{SUS} by closing one pull-up switch before completing a quarter of the ER resonance period, so the discharge current flows through the pull-up switch. Bypassing the discharge current decreases ohmic loss on the ER current path but increases hard-switching loss in the pull-up switches. The hard-switching loss increases with PL because the SUS_UP state starts earlier when PL is heavy than when it is light; this loss degrades the power efficiency.

This paper presents a power-efficient drive circuit for PDPs. The circuit combines all previous methods of reducing PDP power consumption and improves the power efficiency by using two additional techniques: varying the ER inductance, and soft-switching the pull-up switches. The circuit has two separate ER paths to vary the ER inductance in accordance with PL. The ER inductances are L_1 for one path and $L_2 < L_1$ for the other. The ER path with L_1 operates at low PL, the other operates at medium PL, and both operate at high PL. To reduce the hard-switching loss of the pull-up switches, the circuit uses two soft-switching

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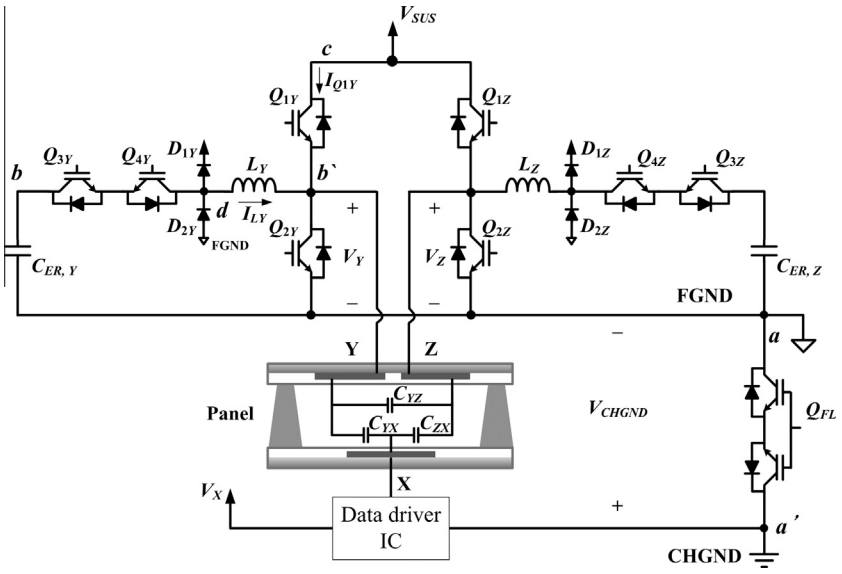

Fig. 1. Schematic diagram for the conventional sustain circuit. FGND (node a): ground for sustain circuit; CHGND (node a′): ground for data drive circuit; electrodes Z, X, and Y: common, data, and scan electrodes, respectively.

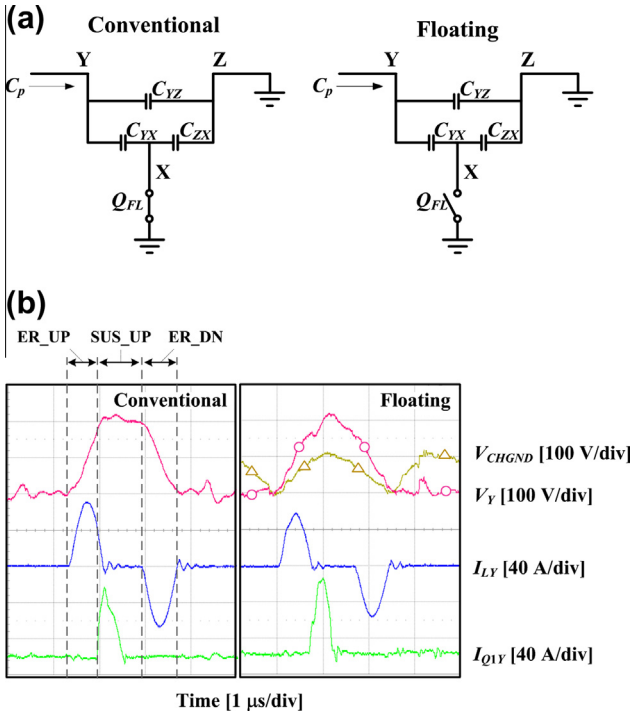

Fig. 2. (a) Equivalent circuit model of the PDP panel and (b) measured sustain voltage and ER current waveforms for the conventional (left) and floating sustain (right) methods.

inductors connected between the pull-up switches and the V_{SUS} source. Various methods of saving PDP power consumption are summarized in Section 2, the proposed circuit is described in Section 3, and the experimental results on a 50″ full-HD PDP are given in Section 4. A conclusion is given in Section 5.

2. Methods of reducing PDP power consumption

For a PDP that uses the address-display-separated method [12], some power is consumed during the address period because the charging/discharging current to X electrodes flows through the data drive circuit. This power loss can be reduced by using an energy recovery circuit [13] and by decreasing the data voltage V_X [2]. The addressed picture is displayed during the sustain period, so considerable power is consumed during this period. This power consumption consists of reactive power consumption which is power loss caused by charging and discharging the panel capacitance, and discharge power consumption which is required to display the picture by inducing glow discharge. Reactive power consumption is important when the picture load is low, and discharge power consumption is important when PL is high. Discharge power consumption occurs in the panel and on the pull-up switches, so it can be reduced by soft-switching the pull-up switches.

2.1. Reactive power consumption

The source of reactive power consumption in a PDP drive circuit is the ohmic loss in the ER path. In a series resonant ER circuit (Fig. 1), the ER current i_L is given by

$$i_L(t) = \frac{V_{SUS}}{2}\sqrt{\frac{C_p}{L}}\sin\left(\frac{t}{\sqrt{C_pL}}\right), \quad (1)$$

where $L \equiv L_Y = L_Z$. Ohmic loss for a given ER path resistance R is proportional to i_L^2, so this loss can be reduced by decreasing C_p or by increasing L; in floating sustain method, C_p is decreased [2] by separating CHGND from FGND for the sustain period, and in the current injection method, L is increased.

2.1.1. Floating sustain method

The floating sustain method was proposed originally to suppress the facial discharge between X and Y, and between X and Z, during the sustain period [2]. In Fig. 1, FGND can be separated from CHGND by switching off the floating switch Q_{FL}. The panel capacitance C_p changes from $C_{YZ} + C_{YX}$ to $C_{YZ} + C_{YX}/2$ when Q_{FL} is switched off, so the floating sustain method can be used to reduce the reactive power consumption (Fig. 2a).

The sustain voltage and current waveforms for the conventional and floating sustain methods were measured at L = 400 nH and V_{SUS} = 200 V on a 50″ full-HD experimental PDP from LG electronics

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