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Asynchronous control of modules activity in integrated systems for reducing peak temperatures

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Abstract

The paper describes a new control method of integrated circuit (IC) modules activity in a modern processor design. The control method leads to improved frequency ability of integrated systems. The proposed solution, based only on computing flow modification, could be easily integrated into all future designs, ranging from a portable computing to a multi-core computing. A new approach to the thermal control method is described along with simulation results. An example of incorporation in current and future integrated circuits into mainstream designs is presented with exemplary algorithms and final simulation results.

Keywords: Asynchronous control; Temperature reduction; VLSI; Microprocessors

1. Introduction

Current research emphasizes that mobile systems are going to be a major player in future production plans [1]. Most consumer electronic top trend products are portable devices. Users need new technologies, commonly available. The global Internet network only emphasizes this trend. It is obvious that current demand for computing power rises every year [2]. For example, those technologies are needed in: multimedia streaming delivery, cryptography, computer graphics (e.g. Transform & Lighting), physics computing (e.g. Havok Physics/Complete) [3], etc. The said premises have led to intensive research efforts in the fields of power supply units [4] and improvements in the integrated circuits' (IC) design.

This article presents a new control method of integrated circuit modules activity in a modern processor design. The control method leads to improved frequency ability of integrated systems. The proposed solution, based only on computing flow modification, could be easily integrated into all future designs, ranging from a portable computing to a multi-core computing.

The exponential dependence of reliability on temperature is the reason for favoring lower operating temperatures [6], and that is why Viswanath et al. noticed that a reduction in temperature only by 10–15 °C can extend the lifespan of a device by as much as a factor of two [5]. The method presented in this paper could lead to minimize the maximum peak temperature of an integrated circuit.

1.1. Power consumption limiting

For example, the Intel Centrino/AMD Mobile and other mobile designs lead to minimization of power consumption [8,9]. This trend has clear drawbacks. Power consumption limiting leads to a decrease in the computation power. Current methods of limiting power consumption could be put into three categories: dynamic frequency scaling (DFS), dynamic voltage scaling (DVS) and dynamic clock throttling (DCT).

Variants of frequency and voltage scaling along with clock throttling could lead to a significant minimization of power consumption [16]. For example, Pentium M processors utilize two methods at the same time [22].

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Voltage and frequency are scaled together to achieve reductions in energy per computation. Scaling frequency alone is insufficient because, while reducing the clock frequency, the processor power consumption is not reduced; the computation execution time is to the first approximation linearly dependent on the clock frequency, and the clock frequency reduction can mean that the computation takes more time and consume the same total energy. Because power consumption is quadratically dependent on voltage level, scaling the voltage level proportionally along with the clock frequency offers a significant total energy reduction while running a processor on a reduced performance level. Many algorithms were designed to control the voltage and the frequency in modern processors. The voltage scaling technique was researched into many publications [10,15,17,20,23–26,30]. The frequency scaling was also considered as a mechanism to minimize the power consumption [13, 21,27]. Research into an extreme usage of electronics (e.g. an extraterrestrial exploration) [7,29] and attempts made at power control on the algorithm level [14,19,28] have also exerted good influence on research effects in this field.

The power needed for a computing effort is tightly connected with the chip temperature. Controlling power dissipation is one way to achieve a proper working temperature. This article presents another method, which is based on a combination of voltage scaling and schedule algorithm modification.

1.2. Processors design trends

Nowadays, the design of common usage processors are similar. Frequency war has no big impact on new processor releases. Current design concentrates rather on concurrent computing than on increasing computation power by a higher working frequency. Dynamic power is tightly combined with the working frequency, and in portable designs it is the most obvious design show-stopper [18]. The same problem arises in a mainframe consist of many multi-core processors. The power consumption is the main problem nowadays. Blade designs [11] consist of many small and independent computing processors incorporated into a small chassis. Power consumption of normal consumer processor (Dual/Quad Core, Athlon, etc.) is too high for this solution. In these fields thermal management plays the main role in the industrial scale application.

Based on the presented general usage processor specifications, it can be seen that the silicon structure is going to be more regular than ever before. The processor design trend is going to isolate functional blocks. Computing modules which appear as general purpose processors are as universal as possible. There is no functional specialization over all blocks. The modules are placed regularly on the chip surface (see Fig. 1 and 2). With this design principle, a modification to the dynamic clock throttling method along with dynamic voltage scaling can lead to interesting results.

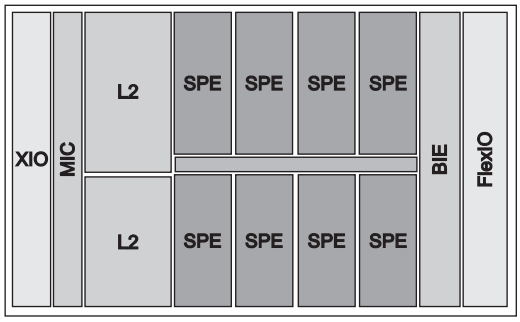

Fig. 1. Current CELL processor design.

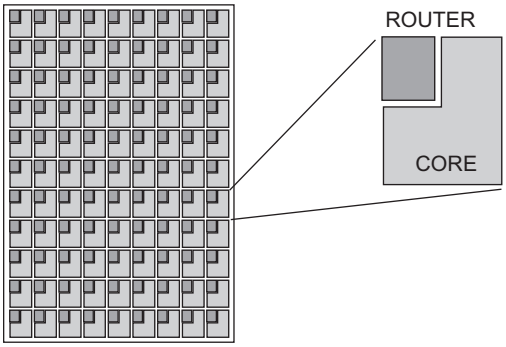

Fig. 2. Future design of Intel 80 cores processor (proposed in production for 2009) [31].

2. Asynchronous control of blocks activity

Asynchronous control of integrated circuit functional blocks activity is based on two power saving methods: dynamic clock throttling and dynamic voltage scaling. Let us make a few assumptions:

- New integrated circuits (e.g. processors) gain a universal applicability model.
- Integrated circuits have got many (N) modules of the same function.
- It is possible to switch selectively between an active module by limiting voltage and/or active clock signals in unused modules.
- It is possible to control the module switching activity by a specialized tracking software installed on the control level in the integrated circuit. The control level consists only of a simple control mechanism which activates/deactivates computation modules.

A functional block is an independent unit of the digital integrated system, e.g. memory, CPU, D/A/D converter, etc. A functional block is in active state if it dissipates dynamic and static energy. The block remains inactive if it dissipates only static energy. Switching activity is defined as a change from active to inactive state or vice versa.

Let us assume a simple model. Few modules are placed on a chip dye (Fig. 3). Functions for blocks are the same. Control modules, memory access, etc. are omitted in this example. A streaming computation (like a multimedia