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A new COP bonding using non-conductive adhesives for LCDs driver IC packaging

Zhi Gang Chen, Young-Ho Kim *

Division of Materials Science and Engineering, Hanyang University, 17 Haengdang-dong, Seongdong-Gu, Seoul 133-791, South Korea

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Abstract

In this study, attempts were made to develop a reliable and low cost chip on plastic (COP) bonding process by using electroplated Sn bump and non-conductive adhesives. Results showed that the bumped chip was successfully bonded with PES, and the initial average contact resistance was less than 30 mΩ, which is much lower than that of ACF bonding. Thermal cycling (TC) test was performed to study the reliability of the COP assembly. The joints passed over 1000 thermal cycles without failure. The contact resistance decreased and leveled off during the TC test. 30 μm fine pitch joints were fabricated and electrically tested. Microstructure observation disclosed that interfacial intermetallic compound formed at the Sn/pad interface, indicating a chemical bonding was achieved. EDS analysis showed that its average composition was very close to $(Cu, Au)_6Sn_5$. During thermal cycling, the interfacial IMC layers were observed to gain dramatic growth.

Keywords: Flip chip; Fine pitch; Non-conductive adhesives; Plastic substrate; Thermal cycling

1. Introduction

As the consumer electronics tends to become lighter, thinner, and also featured in high resolution and lower power consumption to satisfy the increasing market requirements, the trend to use thinner glass substrates in LCDs is propelling. However, as the glass is thinner, the manufacturing cost tends to be higher, partly due to the increase of materials cost, and also it makes the electronic device more fragile, especially under the pressure exerted during the packaging, which would unavoidably lower the production yield. Comparatively, plastic LCDs (PLCDs) with film substrates are found to have a huge market prospect, since it is durable, flexible, unbreakable, and its thickness can be reached below 0.05 mm [1]. It has only 1/6 the weight of a glass substrate [2], which means it is noticeablely lighter. On the other hand, the ever-growing demands for higher and multiple performance of electronics products has given rise to demanding requirements for finer features. This need for high-density interconnect is driving the industry with pitch size of 25 μm or lower [3]. Anisotropic conductive film (ACF) has been used as a dominating adhesive material in the chip on plastic (COP) and COG (chip on glass) bonding [4]. The electrical connection was realized by the intermediate contact via conductive particles squeezed between bumps and pads. However, in fine pitch application below 30 μm, the conductive particles in the space between adjacent bumps easily lead to bridge-shorting. Recently, prevailing interests and extensive investigations have been paid on the non-conductive adhesives (NCAs) applied COG process [5–7]. Instead of reckoning on the mediate connection through conductive particles, this process realizes the direct electrical contact and thereby increases the contact area, which is supposed to lower the contact resistance. It also featured in simple process, cost down and fine pitch feasibility. COP technique is one of the recently developed and well prospective flip chip technologies, which is expected to be capable of meeting the requirements of high-density assembly. As flexible substrate, polyether sulfone (PES) has good high temperature resistance. Its excellent resistance to hydrolysis and dielectric property are also attractive. Compared with glass substrate, PES has water absorption inclination.

Conventionally, gold bumps are popular in the industry. They own good deformation ability and excellent oxidization resistivity. But, gold is precious metal; its high cost fails to satisfy the increasing need for low cost flip chip technology. Sn bumps have smaller hardness, and it is much lower than that of Au bumps and Cu bumps [3], which can be interpreted as

* Corresponding author. Tel.: +82 2 2220 0405; fax: +82 2 2293 7445.
E-mail address: kimyh@hanyang.ac.kr (Y.-H. Kim).

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superior plastic deformation capability. Also, the cost of Sn itself is rather desirable compared with Au bumps.

This study is aimed to develop a low cost, low temperature and fine pitch COP bonding process for the application of LCDs driver IC packaging on plastic substrate. To fulfill low temperature bonding, a commercial NCA that can be cured below 100 °C was utilized. Electroplated Sn bumps were employed as connectors considering its superior deformation capability to compensate for the bump ununiformity, as well as its low manufacturing cost. Fine feature pattern with 30 μm pitch was designed to accomplish fine pitch bonding. Investigation was made on the bondability and reliability of NCA applied COP interconnection. The microstructural evolution of joints was characterized before and after TC test.

2. Experimental

Ti (50 nm), Cu (1 μm) and Au (50 nm) were sequently deposited on passivated Si wafer as the under bump metallization (UBM) and on PES as pad layers utilizing the DC magnetron sputter. Metal trace on the chip was fabricated through photolithographic and wet etching methods. Sn bumps were electroplated on the metal trace with a seed layer of gold. The plating current density is 10 mA/cm^2. Glastic® PES from I-component Corporation was chosen as the flexible substrate. Table 1 listed the properties of this product. To minimize the thermal impact on the LCD module and flexible substrate, NCAs with low curing temperature and appropriate curing time are preferred. In this study, NCA that can be cured at the temperature below 100 °C was provided by Ajinomoto Company. Table 2 summarized the properties of NCA material. As preliminary test, the pattern with bump size of 100 μm in square was attempted to perform bonding. The number of bumps involved in electrical test is 20 per chip. The average bump height is about 20 μm. The pitch of measured bumps is 600 μm. To fulfill fine pitch requirements, 30 μm pitch pattern was designed. The number of measured bumps and bump height are 18 per chip and 18 μm, respectively. The detailed specifications of test chips were summarized in Table 3. The bonding was performed under 100 MPa at 60 and 100 °C, respectively. Table 4 listed the bonding process parameters. The bonding process began with dispensing the NCAs onto the surface of bumped chip, then PES was placed on it. Under thermal source and pressure, the bumped chip was bonded with PES. Fig. 1 illustrated the bonding procedures. Contact resistance of individual bump was measured by four-point probe method. The pattern design on the chip and measurement approach was demonstrated in previous study [8]. In this approach, the pad layer on the PES substrate is not patterned in that it can provide the electrical path for four-point probe measurement and leave out the flip chip bonder with the precise aligning between bumps and pads. Totally, for the pattern with bump size of 100 μm in square, which was used in the preliminary tests, two and three chips were bonded at 60 and 100 °C and tested, respectively. And, five chips (90 bumps) were involved in contact resistance measurement for 30 μm pitch pattern. Thermal cycling (T/C) tests were performed within the temperatures between 0 and 100 °C (30 min/cycle) to examine the reliability of COP joints. The variation of contact resistance was inspected every 100 cycles. The value of contact resistance larger than 100 mΩ was regarded as failure. The microstructure of joints before and after TC test was characterized through scanning electron microscopy (SEM) and energy dispersive spectrometry (EDS) analysis. Thermogravitational analysis (TGA) was conducted to examine the content of fillers in the NCA. The test was carried out in air atmosphere and the temperature was allowed to increase up to 1000 °C.

Table 1
The properties of Glastic® PES

Glass transition temp. (T_g)	225 °C
Coefficient of thermal expansion (CTE)	6.0×10^5 °C
Water absorption (23 °C, 50% RH)	0.8%
Elastic modulus	2.7 GPa

Table 2
The properties of NCA material

Matrix	Fillers	Viscosity (Pa s)	CTE (10^{-6}/ °C)		T_g (°C)	Dielectric constant @ 1 MHz
			α_1	α_2		
Epoxy	Yes	65	50	80	55	3.5

3. Results and discussion

3.1. Results for patterns with 100 μm bump size in square

3.1.1. Thermal cycling test

The specimens, which were bonded at 60 and 100 °C, respectively, have passed 1000 cycles without failure at the

Table 3
Specifications of test chips with different design pattern

Specification	Pattern	
	100 μm bump size in square	30 μm pitch
Chip size	13.5 mm×13.5 mm	12 mm×6 mm
Bump size	100 μm×100 μm	32 μm×14 μm
Bump height (μm)	20	18
Total bumps	100	902
Measured bumps	20	18
Pitch of measured bumps (μm)	600	30