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Analysis of the dependence of indium–gallium–zinc oxide thin-film transistor properties on the gate interface material using a two-stack gate-insulator structure

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To study the interface effects on the device performance, we fabricated indium–gallium–zinc oxide (IGZO) thin-film transistors (TFTs) with a two-stack gate-insulator structure. The two-stack gate insulator was composed of a thick main insulator and a thin interfacial insulator; the main insulator determines the effective permittivity of the gate insulator, and the interfacial insulator regulates the gate/active interface properties. The a-IGZO TFTs had about 10 $cm^2 V^{-1} s^{-1}$ field effect mobility (μ_{FE}) values and 10^7–10^8 switching ratios. The dependences of μ_{FE} and threshold voltage, V_{TH}, on the channel width to length ratio were different according to the electron affinity, χ, of the interfacial insulator. The contact resistance between the source/drain electrode and the active layer, and the electron-injection barrier height from the active layer to the interfacial gate insulator layer could explain this finding. In this work, we successfully demonstrated the method to distinguish the interface-related phenomena from the insulator permittivity-related phenomena.

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1. Introduction

Indium–gallium–zinc oxide (IGZO) thin-film transistors (TFTs) are increasingly used instead of silicon (Si) TFTs in flat panel displays (FPDs). The production cost of IGZO TFTs is similar to that of amorphous Si (a-Si) TFTs that are mainly used for liquid crystal displays (LCDs). In addition, IGZO TFTs have sufficient field-effect mobility (μ_{FE}) values to substitute for poly Si (p-Si) TFTs in organic light-emitting diode (OLED) display applications [1–3]. Due to their low production cost and superior performance, IGZO TFTs are expected to surpass Si-based TFTs in the near future.

Despite the recent commercialization of IGZO TFT-driven display products, the device performance of IGZO TFTs requires further improvements. Display products are evolving to have larger size and complex functions, and demands placed on TFT performance are greater than ever. Current IGZO TFTs do not meet the performance requirements to completely replace Si TFTs, as the μ_{FE} value [2,4,5] for IGZO TFTs reaches only a few tens of $cm^2 V^{-1} s^{-1}$ in comparison with p-Si TFTs, in which μ_{FE} typically exceeds 100 $cm^2 V^{-1} s^{-1}$.

Active layer optimization is one way to improve TFT performance. IGZO active layer material composition and fabrication processes have been studied extensively [6–8]. Further improvement of IGZO TFT performance by optimizing IGZO active layers is unlikely. TFTs using other high-mobility oxide semiconductors such as indium zinc oxide (IZO) have also been studied [9–11]. Although the switching performance of high-mobility oxide semiconductor TFTs may be higher than that of IGZO TFTs, the overall performance is unlikely to exceed that of IGZO TFTs when considering device stability and fabrication process margins.

Choice of gate insulator is another key factor influencing device performance. High-performance TFTs could be fabricated using a high permittivity gate insulator [12–14]. The large gate-insulator capacitance arising from the high-permittivity gate insulator increases the accumulated channel-carrier density and enhances the switching capability. Besides permittivity, other properties of the interface between the active layer and gate insulator can also have a critical influence on device performance, and a precise understanding of the effect of the interface on device properties is essential for improving device performance. However, accurate analysis of interface effects is difficult as they are not easily distinguished from permittivity effects (Fig. 1(a)).

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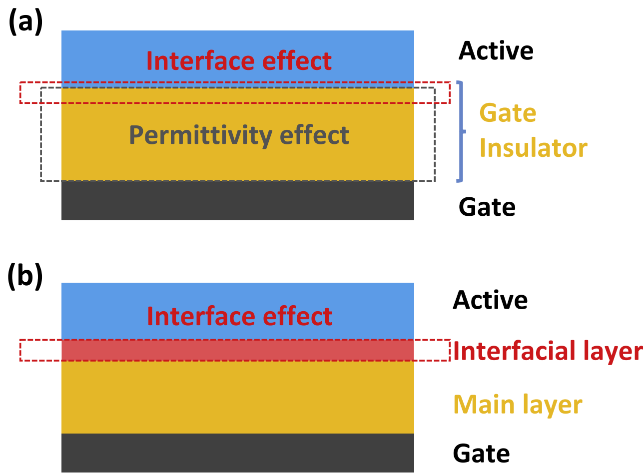

Fig. 1. Schematics illustrating (a) the mixing of interface effects and permittivity effects, and (b) the separation of interface effects from permittivity effects.

Here, we adopt a two-stack gate-insulator structure to separate interface effects from permittivity effects. The gate insulator consists of a main layer and an interfacial layer. The main layer, consisting of a fixed material, occupies most of the gate insulator thickness, and the interfacial layer, composed of a range of materials, occupies a small part of the gate insulator thickness (Fig. 1(b)). Using this approach, we can vary interface properties while maintaining a nearly constant effective permittivity in the gate insulator. The device performance dependence on the interfacial layer is presented and analyzed in subsequent sections.

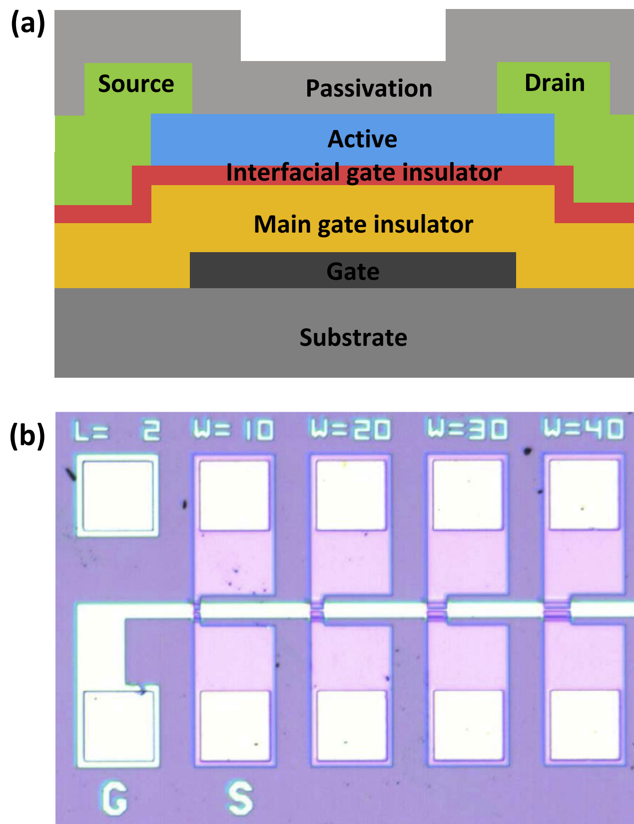

Fig. 2. (a) A schematic illustrating the device structure, and (b) optical micrographs of the fabricated IGZO TFTs.

2. Experimental procedure

Bottom-gate top-contact TFTs were fabricated using IGZO active layers and two-stack gate insulators on oxidation Si wafer substrates (Fig. 2(a)). The gate electrode consisted of a 100-nm-thick Mo layer sputtered on an oxidation Si wafer and patterned using a photolithography method. The main gate insulator consisted of a 100-nm-thick SiO_2 layer deposited by plasma-enhanced chemical vapor deposition (PECVD) at 300 °C on the gate electrode. A 20-nm-thick interfacial insulator was deposited on the gate insulator. In this work, five dielectric materials (SiO_2, Al_2O_3, Si_3N_4, HfO_2, and ZrO_2) were used as the interfacial insulator. Al_2O_3, HfO_2, and ZrO_2 were deposited using atomic layer deposition (ALD) at 150 °C, while SiO_2 and Si_3N_4 were deposited using PECVD at 300 °C. The active layer consisted of 50 nm of IGZO deposited using radio frequency (RF) magnetron sputtering at room temperature with a mixed sputtering gas of Ar:O_2 (100:1 sccm). The source/drain electrode consisted of a 100-nm-thick Mo sputtered layer, patterned using dry etching. The channel surface was treated with N_2O plasma [15–17]. Then, without a vacuum break, a 200-nm-thick SiO_2 passivation layer was deposited at 150 °C using PECVD. Electronic characteristics for the fabricated IGZO TFTs (Fig. 2(b)) were measured using a semiconductor parameter analyzer (HP 4145b) in a dark shielding box at room temperature.

3. Results and discussion

The relative permittivity of the interfacial gate insulator, ϵ_i, was in the range 3.9–25 [18] (Table 1). The effective relative permittivity of the gate insulator, ϵ_{eff}, is related to ϵ_i and the relative permittivity of the main gate insulator, ϵ_m, as

$$\epsilon_{eff} = \frac{\epsilon_m \epsilon_i (t_m + t_i)}{\epsilon_m t_i + \epsilon_i t_m}, \quad (1)$$

where t_m and t_i are the thicknesses of the main gate insulator and the interfacial gate insulator, respectively. Varying the interfacial gate-insulator material may change the interface properties, while the ϵ_{eff} value was nearly fixed in the range 3.9–4.5. All IGZO TFTs demonstrated adequate switching ratios (on current/off current) of 10^7–10^8 (Fig. 3), regardless of the interfacial insulator material used.

μ_{FE} and threshold voltage, V_{TH}, values were extracted from the transfer curves using a linear-mode gradual-channel approximation:

$$I_D = (W/L) C_G \mu_{FE} (V_{GS} - V_{TH}) V_{DS}, \quad (2)$$

where I_D, W, L, C_G, V_{GS}, and V_{DS} are the drain current, channel width, channel length, gate-insulator capacitance per unit area, gate-bias voltage, and drain-bias voltage, respectively. V_{DS} was fixed at 1.0 V to ensure linear mode operation and V_{GS} was swept in the range −10 to 10 V.

For SiO_2 and Al_2O_3 interfacial gate insulators, μ_{FE} decreased monotonically with the W/L value (Fig. 4). For ZrO_2 and HfO_2 interfacial gate insulators, μ_{FE} increased with the W/L value for $W/L < 50$ and then decreased again for $W/L > 50$. For the Si_3N_4 interfacial gate insulator, the dependence of μ_{FE} on W/L was intermediate between the two previous cases.

Table 1
Relative permittivity and electron affinity values for interfacial insulator materials.

	SiO_2	Al_2O_3	Si_3N_4	HfO_2	ZrO_2
Relative permittivity	3.9	9	7	25	25
Electron affinity (eV)	0.9	1	1.6	2.5	2.5

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