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Fabrication of Graphene Field-effect Transistor with Field Controlling Electrodes to improve f_T

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ABSTRACT

In this letter, we report on the fabrication and DC/RF characterization of a novel Graphene Field-effect Transistor (GFET) with two additional contacts at the access regions. The additional contacts—Field Controlling Electrodes (FCEs), are capacitively coupled to the ungated access regions and independently biased to control the access resistance. The reduced access resistance resulted in an increased current-gain cutoff frequency (f_T). The fabricated proposed device could be used for radio frequency (RF) applications.

1. Introduction

The advantages of Graphene as a channel material of FETs include but not limited to its perfect 2D confinement of carriers, high carrier mobility, mechanical flexibility, extremely high thermal conductivity and long phonon mean free path [1,2]. As Graphene is a zero bandgap material, there is no separation or forbidden states between Graphene's valence band and conduction band. In case of a conventional semiconductor material with nonzero bandgap (e.g. Silicon with a bandgap of 1.1 eV), electrons at the valence band need to gain energy equal to or more than the material bandgap to jump up to conduction band, thus contributing in electrical conduction. For transistors made of these materials, it is possible to cease the electron flow from valence band to conduction band by applying suitable gate bias, thus ceasing the channel current. The negligible current still passing through the channel in this condition is termed as off-state current. This small off-state current makes the on/off current ration of these devices very high which is important for reliable switching in logic devices. In contrast, due to the lack of bandgap in Graphene, electrons in its valence band can easily go to conduction band, thus contributing in conduction, and its cessation is not possible by applying gate bias. There is a non-zero minimum conduction point in Graphene FETs which can be considered as off-state current. However, this off state current is non-negligible, thus makes the device on/off current ratio unacceptably low for switching in logic devices [3]. On the contrary, significant advancement has been made on Graphene devices for analog applications. The access resistance reduces the transconductance and drain current of FET, in general, and its adverse effect on current-gain, as well as, on current-gain cut-off frequency (f_T) is well known. That is also true for GFET. To utilize the complete advantage of Graphene as a FET channel material, the set of limitations on the high-frequency performance of GFETs, arisen from the access resistances must be eliminated. Improving high frequency performance by reducing access resistance in III-N HFET and GFET has been already reported [4–6,and]. Two Capacitively coupled and independently biased contacts (Field Controlling Electrode, FCE) at the access region can reduce the access resistance of GFET and increase f_T, significantly. If additional bias is applied to the capacitively coupled additional contacts, it induces additional carriers at the access region of the device which effectively reduces the access resistance. The current gain cut-off frequency is inversely proportional to access resistance. Thus by applying additional bias to the additional contacts, the induced additional carriers at the access region effectively increase f_T. The f_T improvement of GFETs due to these additional contacts has been estimated from numerical and analytical calculations in [7,8]. Here we have fabricated the novel structure GFET with two additional contacts at the access region, measured its DC characteristics and current-gain, and compared with same geometry conventional GFET without FCEs.

2. Theory

The schematic of a conventional 3-terminal GFET on SiO_2 with the small-signal equivalent circuit laid on top is shown in Fig. 1. The time a carrier takes to travel from source to drain, termed as delay time,

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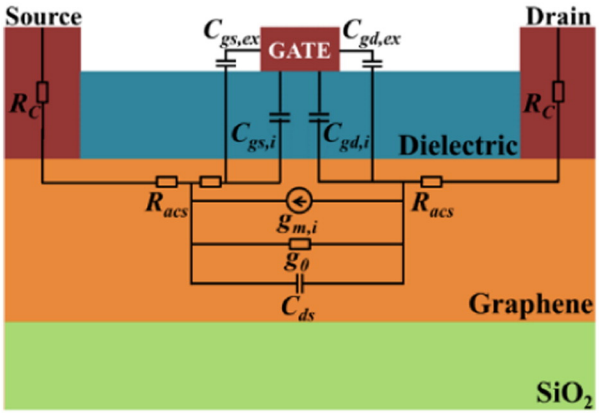

Fig. 1. Schematic of a conventional 3-terminal GFET on SiO_2 with the small-signal equivalent circuit laid on top.

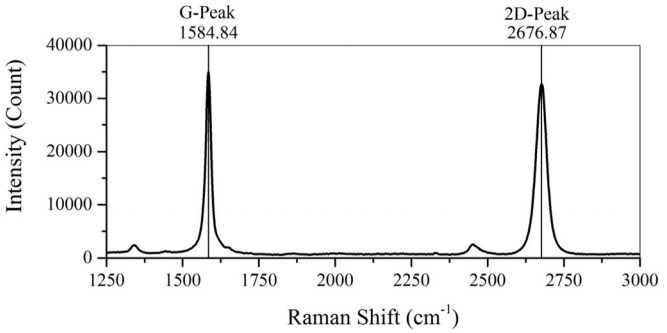

Fig. 3. The 2D/G ratio (0.93) of the Raman spectrum confirms the presence of single layer Graphene forming the device channel.

can be divided into parts: transit delay, τ_{trans} and parasitic delay, τ_{par}. The transit delay is directly proportional to the intrinsic and extrinsic gate capacitance; whereas, the parasitic delay is proportional to the gate capacitances, as well as, on parasitic resistances. The current gain cut-off frequency f_T is inversely proportional to the total delay time in the device and can be expressed as [9]

$$1/2\pi f_T = \tau_{trans} + \tau_{par} \quad (1)$$

As show in [7,8], the induced carriers caused by FCE modulation effectively reduces the resistance of the ungated access regions and thus results in a decrement of τ_{par} and increment of f_T.

3. Fabrication

Rather than following the conventional sequence of GFET fabrication steps starting with Graphene transfer and mesa etch, and ending with gate patterning, here we started the process by firstly pattering gate-FCE on substrate and finished by doing the mesa etch of Graphene, to prevent Graphene from excessive contamination due to exposure to resists, solvents, and developers. The SiO_2 substrate was cleaned with acetone/isopropyl alcohol/methanol, rinsed with deionized (DI) water, and dried with N_2 flow. 200 nm of 950 PMMA A4 was spin coated and oven baked at 185 °C for 30 min. The Gate-FCE layer with alignment marks were patterned using e-beam lithography and developed in a solution of 1: 3 MIBK: IPA. 10-nm Ti/40-nm Au was evaporated using e-beam evaporator at a chamber pressure of 2×10^{-7} mTorr and lifted-off in acetone, in a standard sonic bath. The next layer was the pads for which the patterned substrate was coated with 600 nm LOR 3B/600 nm S1805 photoresist. After UV exposure, it was developed in developer MF-26A for 15 s, rinsed with DI, dried with N_2, and a descum was done by oxygen plasma etching for 15 s. 10-nm Ti/500-nm Ni was evaporated for pad layer metallization and lifted-off. Following the Gate-FCE layer and pad layer formation, 20 nm HfO_2 was deposited by atomic layer deposition (ALD), as gate dielectric. Then it went through the same photolithographic process with mask to open windows for the pads. The 20 nm dielectric above the pads was etched by reactive ion etching (Chlorine + Argon) through the windows, followed by source/drain patterning. For the source/drain patterning, the same e-beam lithographic process was used and 10-nmTi/50-nm Au was evaporated, followed by the same lift-off process in sonic bath. Source-Drain pad layer was patterned by the photolithographic process same as that used for Gate-FCE pad layer, followed by a 10-nm Ti/500-nm Au evaporation, and lift-off.

Single layer CVD Graphene grown on Copper sheet was coated with PMMA using a regular spin coating and was put floating on $FeCl_3$ solution for 8 h without any disturbance while copper surface touching the solution. Once the copper was completely etched, it was washed with DI water multiple times without flipping, and eventually was transferred on the patterned substrate. After transfer, the sample was put in a desiccant for 8 h. Graphene covered with PMMA was then

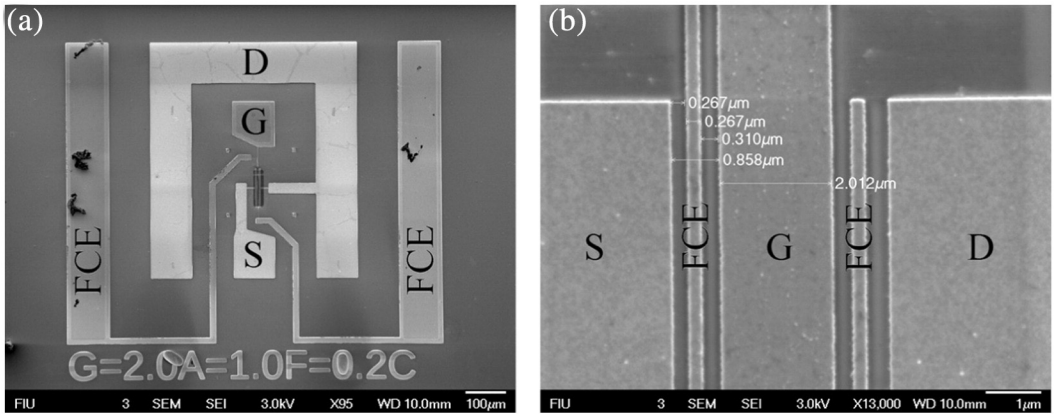

Fig. 2. (a) SEM image of the device at low magnification. (b) High magnification image with embedded scale showing FCE length, gate length, and access region length. The letters S, D, and G represent respectively the source, drain and gate terminal.