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Self-assembly La-rich nanocrystals in metal-gate MIS structures for non-volatile memories

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ABSTRACT

TiN/ZrN/high-κ (ZrLaO)/Si (MIS) structures were fabricated. Localized La-rich oxide behaving like nanocrystal (NC) has been self-formed between ZrN cap and TiN gate metal after 850 °C annealing. The program speed of 1 μs was achieved with capacitance ratio >3. The large C–V memory window of 2 V was observed at swept voltage of ±4 V. TEM analysis shows two discrete regions (NC and metal cap), which leads to two levels of speed sensitive. The endurance properties show small degradation in flatband voltage shift after 10^6 cycles. The relative dielectric constant is 11.1 and equivalent oxide thickness is 7.8 nm.

1. Introduction

Conventional floating-gate nonvolatile memories (NVM), which includes a continuous doped-poly silicon thin film in the SiO_2 gate dielectric as the charge retaining medium, will lose all injected charges when a single path is leaky in the tunnel oxide layer [1]. Recently, nanocrystal (NC) memory devices have attracted much attention due to more aggressive scaling on the tunneling oxide. The benefit of NC embedded SiO_2 structure resolves the above problem because one leaky path in the tunnel oxide only drains charges stored in a few nanodots [2]. The charge loss from the NCs through the tunneling oxide can be localized by the discrete isolation of each NC. Tiwari et al. [3] were the first to demonstrate memory effects using the concept of embedded silicon NCs in the insulator layer. Later, a wide range of metal NC materials, such as Au, Ag, Pt, Ni, and W, has been successfully fabricated [4–8]. In addition, similar to the charge trapping layer of SONOS-type flash memory, high-κ dielectrics can be introduced in NC memories to obtain the purpose of the equivalent oxide thickness (EOT) scaling, the interpoly leakage current reduction, and the field-sensitive tunneling [9]. High-k dielectric materials, such as HfO_2 [10] ZrO_2 [11] Y_2O_3 [12] and La_2O_3 [13] are promising candidates to substitute Si_3N_4 films as the charge trapping layer of SONOS-type memory devices. Such high-k dielectric films can achieve better charge trapping characteristics due to high densities of trap states and deep trap energy levels [14], which leads to a longer retention time [15].

Although the performance of NC memory devices with various sizes and tunnel/control oxide thicknesses has been experimentally developed, the repeatability of NC distribution nature of process and the uniform size is a big challenge. Theoretically, the tunnel oxide in the NC memory device can be reduced to allow faster programming and lower voltage operation, but a high speed less than 1 μs is seldom reported. In contrast, novel SONOS-type and floating-gate devices can achieve 100 ns or even less than 10 ns program speed [16,17]. This is because scaling the tunnel oxide into the direct tunneling regime is easier in order for fast program speed improvement and unlimited endurance of direct tunneling operation. The simple fabrication process, which is fully compatible with CMOS logic, is advantageous as compared to the DRAM for scalable embedded memory [17]. In this study, we follow one of the robust CMOS structures with a metal capping layer on the top of high-k gate dielectric for the purposes of better thermal stability and acting a barrier against oxygen diffusion [18,19]. The NC is self-formed between capping layer and metal gate after a high annealing temperature. In this new architecture, the quality

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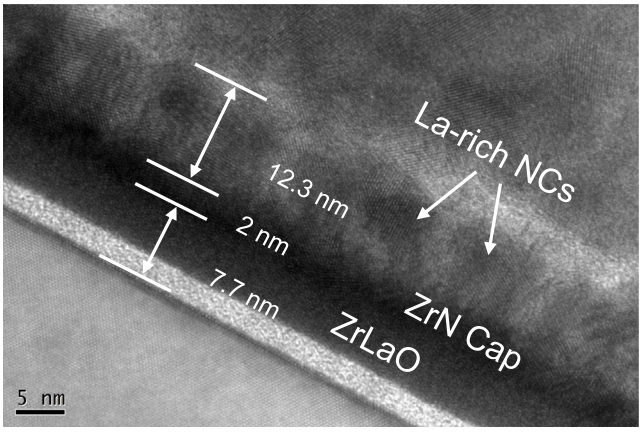
and thickness of tunneling oxide can be well controlled. The EOT scaling down to the current technology node, which exhibits many advantages in electrical and/or physical properties, e.g. process compatibility, high program/erase (P/E) speed, low programming voltage and power consumption.

2. Device fabrication

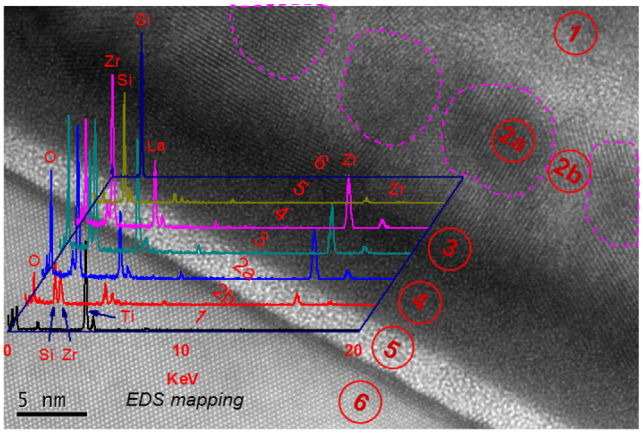
P-type, (1 0 0) orientation, 4-in.-diameter silicon wafers (1–5 Ω-cm) were used as the starting substrates. Standard oxide cleaning ($HF:H_2O = 1:10$) was performed before deposition. The ZrLaO thin films were deposited by cosputtering of ZrO_2 and La targets in mixed argon and oxygen gases at room temperature. The flow rate of argon and oxygen were 20 and 4 sccm (cubic centimeter per minute at STP), respectively. The purities of ZrO_2 and La targets were 99.9% and 99.99%, respectively. The ZrO_2 target used the generation power of 80 W under a radio frequency (RF) of 13.56 MHz and the La metal target used the direct current (DC) powers of 3, 6 or 9 W, simultaneously. The ZrLaO film thickness was kept at 7 nm with the deposition time of 33.3, 28.0 and 24.1 min which corresponds to the deposition rates of 0.21 nm/min (3 W for La), 0.25 nm/min (6 W) and 0.29 nm/min (9 W). To avoid the moisture absorption problem observed at La-doped oxide [20,21], the ZrN capping layer was deposited right after the ZrLaO thin-film finished the process without venting the chamber. TiN was used as the top electrode. The thicknesses of ZrN cap and TiN electrode were 2 and 50 nm, respectively. Postmetallization annealing (PMA) was performed for ZrLaO in pure N_2 at 550, 700, and 850 °C for 30 s. The crystalline phase of ZrLaO thin films was identified by X-ray diffraction (XRD). The characteristics of current–density versus electric-field (J–E) were measured with an Agilent B1500A electrometer and the capacitance–voltage (C–V) measured with an Agilent 4980 LCR meter. High-resolution transmission microscopy (HRTEM; JEOL JEM-2010F) was used to confirm the microstructures of the ZrLaO thin-film and interfacial layer. EDS mapping was investigated.

3. Results and discussion

Fig. 1(a) shows the TEM analysis of uniformly TiN/ZrN/ZrLaO/*p*-Si stack structure after 850 °C PMA. A thin layer with NC embedded is forming on the top of metal cap/high-k stack as compared to no obvious NC formed in the same structure at lower annealing temperature of 550 °C (not shown here). The image indicates the thickness of this layer is about 12 nm with 5 nm diameter size of NCs. Fig. 1(b) shows the EDS mapping of the TiN/ZrN/ZrLaO/*p*-Si structure. The outdiffusions of oxygen and silicon have been identified at this interfacial layer between TiN and ZrN. The oxygen atom is from the dielectric layer, whereas the silicon atom is from the silicon substrate. Relatively high amounts of oxygen and/or silicon atoms at this self-forming layer are because of surface oxidation. Considering the Gibbs free energy of formation for the oxide (ΔG^0_{ox}), the dominant reaction is the oxidation of TiN surface layers due to $\Delta G^0_{ox} = G^0_{TiO_2} - (G^0_{Ti} + G^0_{O_2}) \sim -725$ kJ/mol at 850 °C [22]. Si atoms (or volatile SiO gas) take oxygen atoms out of Ti–O and Ti–ON bonding states in the TiN metal electrode with high-temperature annealing, resulting in the formation of SiO_2 compounds, which was confirmed by Rutherford backscattering spectroscopy (RBS) and core-level photoemission spectroscopy [23]. However, the thermodynamic reactions of silicide formation: $TiO_2 + 3Si = Si_2Ti + SiO_2$ and/or $TiO_2 + 2Si = SiTi + SiO_2$ are more favorable processes instead of redox replacement: $TiO_2 + Si = Ti + SiO_2$ due to overwhelming difference in Gibbs free energy [24]. High ratios of Zr and La have been found in the region of 2a, but only the LaO phase of crystallization peak is observed at Fig. 2. It can be



(a)



(b)

Fig. 1. TEM analyses of TiN/ZrN/ZrLaO/*p*-Si structure after annealing at 850 °C with (a) the cross-sectional TiN/self-formed NC layer/ZrN capping layer/high-k/Si stack. (b) The EDS mapping plotted at locations of 1–6 regions. 2a and 2b are with NC and without NC in the same layer, respectively.

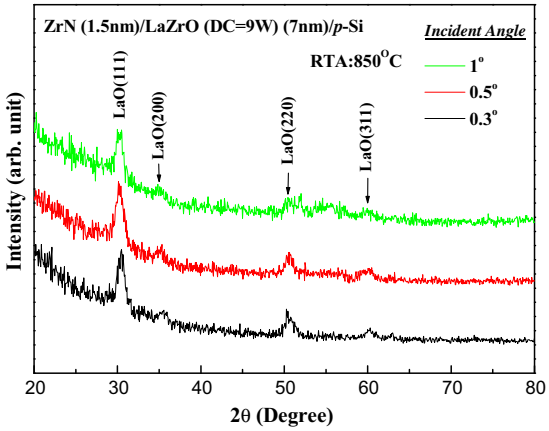


Fig. 2. XRD patterns of ZrN/ZrLaO/*p*-Si structure at different incident angles of 1°, 0.5°, and 0.3°.

explained that the needed oxygen pressure to stabilize the binary oxides is in the order of $SiO_2 > TiO_2 \gg ZrO_2 > La_2O_3$, which means that a pressure of 10^{-45} Torr O_2 is sufficient to form a stable La_2O_3 at oxygen-deficient condition compared to 10^{-40} Torr for