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Thickness dependence of $Al_2O_3/HfO_2/Al_2O_3$ stacked tunneling layers on gadolinium oxide nanocrystal nonvolatile memory

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ABSTRACT

Characteristics of Gd_2O_3-NC memories with multiple tunneling layers of $Al_2O_3/HfO_2/Al_2O_3$ (AHA) have been investigated. It can be found that the Gd_2O_3-NC memory with thin bottom and thin top Al_2O_3 film of AHA stacked tunneling layers exhibits superior programming and erasing (P/E) properties, respectively. Compared with the memory with SiO_2 tunneling layer, the retention characteristics of Gd_2O_3-NC memories with AHA stacked tunneling layers are significantly improved. In addition, for the memories with AHA stacked tunneling layers, the trapping energy level (E_t) of shallow-trap (ST) electron loss is decreased but that of deep-trap (DT) electron loss is increased due to some shallow traps within HfO_2 film and the midgap interface states at HfO_2/Si interface respectively. Further, the dependence of AHA stacked layer thickness on memory characteristics can be explained by the band engineering of tunneling layer. The Gd_2O_3-NC memories with AHA stacked tunneling layers can sustain a stable memory window of more than 1.6 V after a P/E cycling test of 10^4 times.

1. Introduction

Nonvolatile memories with floating gate (FG) structure have encountered a serious bottleneck owing to the limitation of tunneling oxide scaling and significant cell-to-cell coupling effect [1–4]. The data retention of FG flash memory is dramatically degraded when the tunneling oxide shrinks to a certain thickness. Recently, the discrete charge storage concept has been demonstrated to replace the conventional FG flash memory [5,6]. One method is to apply the charge-trapping flash (CTF) memory such as the silicon–oxide–nitride–oxide–silicon (SONOS) structure, which has been discovered by Wegener in 1967 [5]. The performance can be further enhanced by using the bandgap-engineered SONOS (BE-SONOS), where the multiple tunneling layers, $SiO_2/Si_3N_4/SiO_2$ (ONO), have been implemented [7–10]. The charge loss can be reduced due to the thick ONO tunneling layers, while the carrier injection efficiency can be kept as the conventional SONOS flash memory by using the band engineering technique. Moreover, it is reported that the programming and erasing (P/E) speed is mainly dominant by the bottom SiO_2 film of multiple tunneling layers only because the programming and erasing mechanism of SONOS flash memory is proposed to be hot electrons and hot holes injection, respectively [10].

The other method is using the isolated nanocrystals (NCs) such as Si, Ge, Au, and HfO_2, as storage islands which can effectively reduce the lateral migration of charges, thereby improving the memory characteristics [6,11–13]. Furthermore, the gadolinium oxide (Gd_2O_3) nanocrystal, a rare earth metal oxide material, has been proposed to exhibit superior memory properties [14–19]. The Gd_2O_3-NCs can be formed by the crystallized Gd_2O_3 dots with small band-gap surrounded by the amorphous Gd_2O_3 film with large band-gap [20], which is different from the traditional NCs embedded in SiO_2 matrix [6,11–13]. It is reported that the CF_4 plasma treatment on Gd_2O_3 film can achieve a band engineered NC memory with improved memory behaviors [16,17]. The CF_4 plasma treatment for a long time with significant plasma damage will degrade the memory performance. In addition, the memories with hybrid Gd_2O_3 nanocrystal and charge trapping layer have been realized by using a thick Gd_2O_3 layer [18]. Though the memories with thick Gd_2O_3 layer presented enhanced memory characteristics, the endurance property was found to be degraded due to the charge trapping issue. Unfortunately, the charge loss of Gd_2O_3-NC memories is still serious especially for the high temperature operation. To further enhance the P/E efficiency and data retention properties, the Gd_2O_3-NC memories with HfO_2/Al_2O_3 nanostructure tunneling layers have been proposed [19]. In this work, an additional Al_2O_3 film has been included to form the $Al_2O_3/HfO_2/Al_2O_3$ (AHA) stacked tunneling layers of Gd_2O_3-NC memories. By the bandgap-engineering of AHA stacked tunneling

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layers with different top and bottom Al_2O_3 thicknesses, the enhanced programming and erasing properties can be achieved by the Gd_2O_3-NC memories with thin bottom and top Al_2O_3 film, respectively because of the different carrier injection polarities. Furthermore, the trapping energy levels of Gd_2O_3-NC memories with AHA stacked tunneling layers are extracted and found to be influenced by the thickness of $Al_2O_3/HfO_2/Al_2O_3$ layers.

2. Experimental procedures

The Gd_2O_3-NC memory devices were fabricated on 4 inches n-type (100) silicon wafers. First, the Radio Corporation of America (RCA) cleaning was performed and followed by the deposition of 1 and 2-nm-thick Al_2O_3 film on silicon wafers by radio frequency (RF) sputtering with a 99.99% pure aluminum (Al) target. Next, a 5-nm-thick HfO_2 layer was deposited by the atomic layer deposition (ALD) with the precursor of tetrakisethylmethylaminohafnium (TEMAH) and water. Then, a 2 to 4-nm-thick Al_2O_3 film was deposited by the RF sputtering. The samples with the thickness of multiple $Al_2O_3/HfO_2/Al_2O_3$ (AHA) tunneling layers for 0 nm/5 nm/4 nm, 1 nm/5 nm/3 nm, and 2 nm/5 nm/2 nm were denoted as S1, S2 and S3, respectively. All samples were then rapid thermal annealed at 800 °C for 30 s in N_2 ambient to reduce the traps within the AHA layers. In addition, a 4-nm-thick SiO_2 film was thermally grown on a silicon wafer by furnace in O_2 ambient, which was fabricated for comparison and denoted as C. After that, an 8-nm-thick Gd_2O_3 layer was deposited by using the RF sputtering with a 99.9% pure gadolinium (Gd) target in argon (Ar) and oxygen (O_2) mixed ambient at room temperature. The flow ratio of Ar to O_2 was 7:1 under a chamber pressure of 10 mtorr and an RF power of 100 W. After the Gd_2O_3 film had been formed, the samples were subjected to rapid thermal annealing (RTA) at 900 °C for 30 s in N_2 ambient to form Gd_2O_3-NCs [14]. A 10-nm-thick SiO_2 layer was deposited by plasma-enhanced chemical vapor deposition (PECVD) system to act as a blocking oxide. Finally, a 300-nm-thick Al film was deposited by thermal evaporator with a pure Al ingot (99.999% pure), and a gate was defined lithographically and etched. The sample without the Gd_2O_3 layer and with the multiple AHA tunneling layers was also fabricated and denoted as S0. The sample splits with simplified process conditions were listed in Table 1. The schematic memory structure and a high resolution transmission electron microscopy (HRTEM) image of the cross-sectional view of Gd_2O_3-NC memory with AHA stacked tunneling layers (sample S2) were displayed in Fig. 1. From this figure, distinct Gd_2O_3-NCs and AHA stacked tunneling layers can be observed. Further, it can be found that there is a significant interfacial layer (IL) between Al_2O_3 and Si substrate, which is easily formed at the high-k/Si interface [21]. The capacitance–voltage (C–V) curves were measured by using an HP4285 precision LCR meter, and the P/E characteristics were measured by using an HP8110 pulse generator to supply the gate pulse.

Table 1
The sample splits and simplified process flows of Gd_2O_3-NC memories with conventional SiO_2 and multiple AHA tunneling layers.

	S0	S1	S2	S3	C
Gate	Al(300nm) by thermal coater				
Blocking oxide	SiO_2(10nm) by PECVD				
Trapping layer		Gd_2O_3(8nm) by RF sputter			
Tunneling layer	Al_2O_3(2nm) by sputter / HfO_2(5nm) by ALD / Al_2O_3(2nm) by sputter	Al_2O_3(4nm) by sputter / HfO_2(5nm) by ALD	Al_2O_3(3nm) by sputter / HfO_2(5nm) by ALD / Al_2O_3(1nm) by sputter	Al_2O_3(2nm) by sputter / HfO_2(5nm) by ALD / Al_2O_3(2nm) by sputter	SiO_2(4nm) by furnace
Substrate	n-Si				
Backside contact	Al(300nm) by thermal coater				

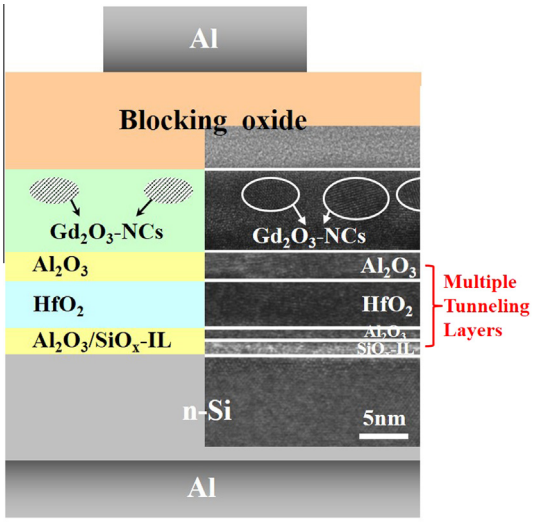

Fig. 1. Cross-sectional structure and HRTEM image of Gd_2O_3-NC memory with AHA stacked tunneling layers. The crystallized phase of Gd_2O_3-NCs surrounded by the amorphous phase can be observed. Note that a silicon dioxide (SiO_2-IL) at Al_2O_3 and Si substrate interface was formed.

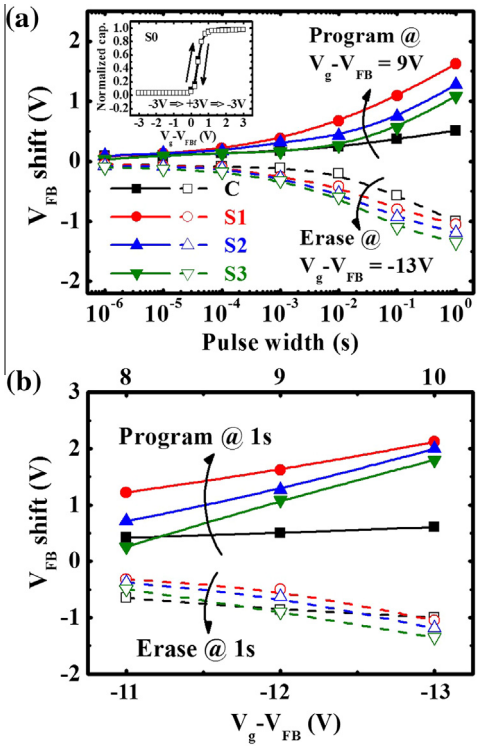

Fig. 2. (a) Flat-band voltage shift versus pulse width characteristics of Gd_2O_3-NC memories programmed at $V_g - V_{FB} = 9$ V and erased at $V_g - V_{FB} = -13$ V. The capacitance–voltage (C–V) hysteresis measured from −3 V to +3 V then swept back of sample S0 was shown in the inset figure. (b) Summarized flat-band voltage shift of Gd_2O_3-NC memories programmed and erased at $V_g - V_{FB}$ of 8∼10 V and −11∼−13 V, respectively for 1 s.