Microelectronic Engineering 138 (2015) 107–110

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Effects of HfO_2/SiON/SiN stacked trapping layer on operation characteristics of poly-Si flash memory devices

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ARTICLE INFO

Article history:
Received 1 August 2014
Received in revised form 30 January 2015
Accepted 21 February 2015
Available online 11 March 2015

Keywords:
Poly-Si
Junctionless
Charge-trapping
HfO_2
Si_3N_4
Flash memory

ABSTRACT

A HfO_2/SiON/SiN (HON) bandgap-engineered trapping layer (BETL) on inversion-mode (IM) and junctionless (JL) polycrystalline-Si flash memory devices is investigated in this work. The HON layer is formed by performing a rapid thermal oxidation process between the depositions of SiN and HfO_2. For IM device, the programming speed, retention and endurance characteristics are improved by the HON BETL while without degrading its erasing speed when compared to that with HfO_2/SiN (HN) BETL. As to the JL device, improved erasing speed and retention characteristics are obtained with HON BETL; high programming speed and good endurance performances of the JL device are also observed. HON BETL is promising to improve retention characteristics of poly-Si flash memory devices since the conduction band level of SiON is higher and the trap density of SiON is lower as compared to those of SiN.

1. Introduction

For the increasing demand of NAND flash memory cells, polycrystalline channel material is becoming attractive for three-dimensional (3-D) integration [1–3]. An advanced junction engineering is necessary since source/drain (S/D) definition and implantation are hardly achieved for 3-D architecture. A "junctionless (JL)" concept is reported to replace the conventional junction formation process by homogeneously doping source, drain and channel [4]; no junction is formed and the fabrication process is simplified. The operation speeds of JL flash memory devices are greatly affected by the channel doping conditions. For n-channel JL flash device with SiN trapping layer, heavier channel doping results in faster programming speed but it sacrifices erasing speed due to its lower hole concentration [5,6]. Bandgap-engineered trapping layer (BETL) is very promising to replace single SiN trapping layer since better operation speeds and reliability characteristics can be achieved by well stacking trapping layer materials with different bandgaps [7–9]. SiN/SiON/SiN BETL and those others with similar band structure are reported to demonstrate improved operation characteristics since the trapped charges are well distributed by a larger bandgap of their middle trapping layer [7–9]. However, most of the BETL studies are based on bulk planar devices. The study of BETL on polycrystalline-Si (poly-Si) channel device is rarely seen and its effects on junctionless device are not yet reported. In this work, effects of HfO_2/SiON/SiN (HON) BETL on the operation characteristics of both inversion-mode (IM) and JL poly-Si flash device are investigated for the first time. Operation characteristics of HON and HfO_2/SiN (HN) BETL on IM and JL poly-Si device are compared as well.

2. Device fabrication

IM and JL flash memory devices are both fabricated on 6-inch Si wafers. The fabrication process of IM and JL nanowire devices is shown in Fig. 1. A 200-nm thick SiO_2 is firstly grown by a low-pressure chemical vapor deposition (LPCVD) system. A 50-nm thick Si_3N_4 buried layer is deposited, followed by an 100-nm thick SiO_2 by LPCVD systems. Four SiO_2 dummy fins with a height of 100 nm are formed by I-line lithography and reactive ion etching (RIE) processes as shown in Fig. 1(a). An 100-nm thick amorphous-Si is then deposited and transferred into poly-Si by solid-phase crystallization (SPC) process at 600 °C for 24 h. Phosphorous implantation (at 30 keV to a dose of 1×10^{13} cm^{-2}) and activation (900 °C for 30 s) are performed on JL samples without any lithography definition. After that, S/D region is defined on two ends of dummy fins for all samples. Eight spacer nanowire (NW) channels are consistently formed by precise RIE process control and connected with naturally raised S/D as shown in Fig. 1(b). SiO_2 dummy fins are removed by diluted HF to complete active region. After a 4.5-nm thick tunneling SiO_2 is grown by a rapid

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http://dx.doi.org/10.1016/j.mee.2015.02.044
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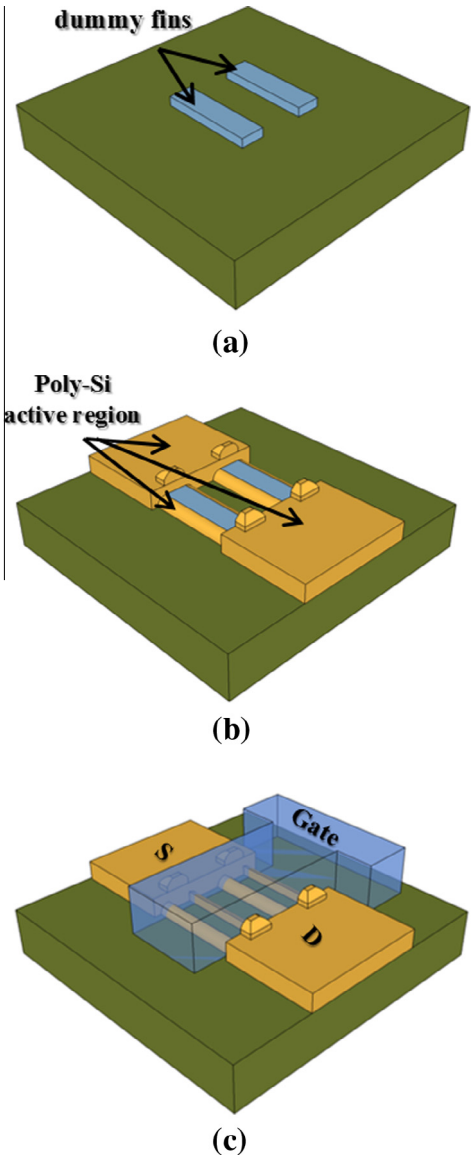

Fig. 1. Schematic fabrication process of IM and JL devices.

thermal oxidation (RTO) process and a 3-nm thick SiN is deposited by a LPCVD system for all samples, some samples are sent to simply deposit a 7-nm thick HfO_2 to form HN BETL by a metal–organic chemical vapor deposition (MOCVD) system. Other samples are sent to perform RTO process at 1000 °C for 30 s for an ultra-thin SiON layer and deposit a 7-nm thick HfO_2 to complete HON BETL. The SiON layer is thermally grown since it is reported to have better interface with SiN when compared to a deposited one [10]. An 18-nm thick Al_2O_3 is then deposited as blocking layer by a MOCVD system; a 300-nm thick TiN is deposited as metal gate by a physical vapor deposition. All samples are defined and etched to form gate region as shown in Fig. 1(c). Phosphorous implantation (at 30 keV to a dose of 5×10^{15} cm^{-2}) and activation (900 °C for 30 s) are performed on IM samples for N^+ doped S/D. Passivation and metallization processes are performed on all samples, followed by sintering at 400 °C for 30 min to complete the device fabrication.

The channel width and length of devices used for characteristic measurements are ~1.1 and ~1.0 μm, respectively. About eight devices of each sample are tested in every measurement. The measured data are shown in average values. Since the data deviation for each sample is little, the uniformity of NW geometry and dielectric thicknesses are quite good.

3. Results and discussion

Fig. 2 shows the cross-sectional transmission electron microscopy (TEM) image of the JL device with HON BETL (JL-HON). An NW width of ~25 nm is clearly observed, which is small enough for JL devices to be turned off. Although the thermally formed SiON is not clear on the TEM image due to the smooth interface of SiON/SiN [10], the effects of HON BETL can still be observed by the electrical characteristics shown later. The total EOT of IM and JL devices are about 15.5 nm, since the k value of Al_2O_3 is 9, Si_3N_4 is about 7.5 and HfO_2 is 18 [11,12].

The transfer characteristics of IM and JL devices at drain voltage (V_{DS}) = 0.5 V are shown in Fig. 3. The JL devices show clear transfer characteristics, which indicates that their doped channels with the NW width of ~25 nm can be effectively depleted. The on-currents of the JL devices are lower than that of the IM ones mainly due to the lower implantation dose of doped channel formation. The on-current of the JL-HON device is a little smaller than that of the JL one with HN BETL (JL-HN). It is because the process temperature during SiON formation leads to dopant segregation and decreases the effective channel doping of the JL-HON device. The erasing speed of JL flash memory device can be enhanced by a lower n-type channel doping [5].

Fig. 4(a) shows the programming speeds of IM and JL devices at gate voltage (V_{GS}) = 15 V. The programming and erasing (P/E) operations in this work are all performed by the Fowler–Nordheim tunneling mechanism. The threshold voltage (V_{th}) shift in Fig. 4(a) refers to the V_{th} of erase state. The programming speed of the IM device with HON BETL (IM-HON) is faster than that with HN BETL (IM-HN), since the SiON energy barrier of HON BETL increases the electron scattering as the band diagram shown in Fig. 4(b). Thus, the programing capture efficiency is improved [8,9]. As for the JL devices, the programming speed of the JL-HON device is similar to that of JL-HN one. Because a very thin SiON in HON CTL is formed from HN by a RTO on Si_3N_4 (N) and then a HfO_2 (H) deposition, the channel doping of HON device is lower than that of HN one due to dopant segregation. Hence, the lower effective channel doping of JL-HON device results in less electron injection as compared to JL-HN one. Although the lower effective channel doping of JL-HON device results in less electron injection [5], the better capture of injected carriers by HON BETL compensates this disadvantage.

Fig. 5(a) shows the erasing speeds at V_{GS} = −15 V. Devices are programmed for 1 s before erasing speed measurement. The V_{th}

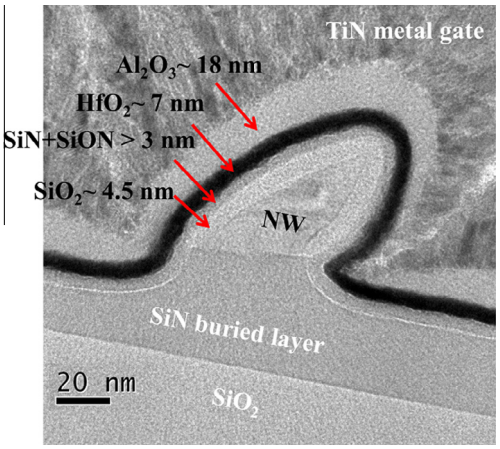

Fig. 2. Cross-sectional TEM image of JL poly-Si flash device with HON BETL.