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Device stress evaluation of InAs/AlSb HEMT on silicon substrate with refractory iridium Schottky gate metal

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ABSTRACT

In this work, the 6-inch AlSb/InAs on Si (001) substrate is used to increase device integration and cost-effective purpose. The iridium (Ir)-gate was used for the InAs/AlSb on silicon substrate and temperature-dependent characteristics were also studied. The Ir-gate exhibited a superior metal work function which was beneficial for increasing the Schottky barrier height of InAs/AlSb on silicon heterostructures. Moreover, transmission electron microscopy, secondary ion mass spectrometry, and low frequency noise measurements were conducted to proof that the Ir-gated AlSb/InAs HEMT achieved the better stability of characteristics after self-heating and hot-carrier stresses.

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1. Introduction

Sb-based devices provide the intrinsic advantages of high-speed and low power consumption that can satisfy the expanding requirements of commercial applications. Much progress in InAs(Sb)/Al(Ga)Sb and In(Ga)Sb/InAlSb HEMTs have been reported and studied [1–2]. The electronic band structure of InAs enables to obtain faster electron transport owing to its lower effective mass ($0.023mo$) in the Γ-valley relative to most of all other common III–V semiconductors, except InSb, and a large Γ–L valley separation (relative to the band gap) of 0.72 eV. Therefore, an excellent electron mobility as high as 20,000–30,000 cm^2/V-s in the InAs/AlSb quantum wells could be achieved [3–4]. The Schottky barrier height (Φ_B) is an important parameter to improve the signal dynamic range and to reduce the gate leakage current of InAs/AlSb HEMTs. For E/D-mode digital IC design, high Φ_B design of Sb-based HEMT is also beneficial to have a large Schottky barrier height to increase the logic noise margin. Traditional Pt or Ti gate metal design performed the Φ_B values around 0.5–0.55 eV. However, the diffusion or penetration of these metals during long-term operation, which lead to a device reliability problem, has prevented this technology from receiving wide attention. Ir was hence investigated as the Schottky gate metal of InAs/AlSb on 6-inch Si substrate owing to its high work function (5.27 eV) together with a high melting point of 2450 °C and these characteristics imply this metal could provide high Schottky barrier and good thermal stability [5]. In this study, we first demonstrates the stabilities of DC characteristics and low frequency noise performance of InAs/AlSb HEMT using Ir-gate on a silicon structure with a 5 min stress evaluation. The temperature dependent g_m degradation slope of device is −0.44 mA/mm K and this slope is −0.17 mS/mm K of device current temperature-dependent variation. The device stable output characteristics with various temperature operations indicated that the iridium refractory Schottky gate metal is very suitable for using as antimony compounds gate electrode. Therefore, Ir-gate technology for the InAs/AlSb HEMT on silicon substrate has great potential for cost-effective and high speed ICs applications.

2. Device structure and fabrication

The InAs/AlSb HEMT epitaxial was grown by solid source molecular beam epitaxy (MBE) on a 6-inch semi-insulating silicon (001) substrate. The conventional GaAs on Si migration enhanced growth (MEE) epitaxy method was adopted to be the first buffer seed layer. Between the AlSb/AlGaSb/AlSb composited back barrier layer and GaAs MEE seed layer, the graded GaAsSb composited layers were grown to release the strain induced by the large lattice mismatch of 11% between the AlGaSb and the Si substrate [6]. Then the 13 nm AlSb Schottky layer was grown on the 8 nm InAs channel to form the two dimensional gas (2-DEG) quantum well channel. Finally, the InAlAs/InAs layer located on the AlSb Schottky layer

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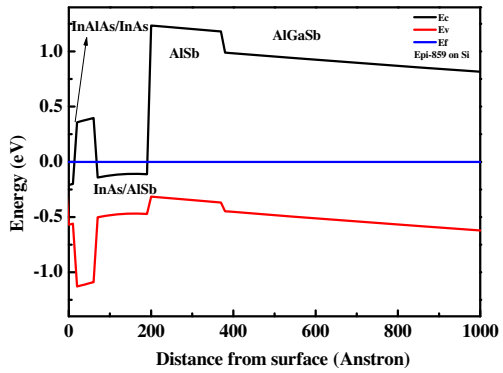

Fig. 1. The energy band diagram of InAs/AlSb HEMT on silicon substrate.

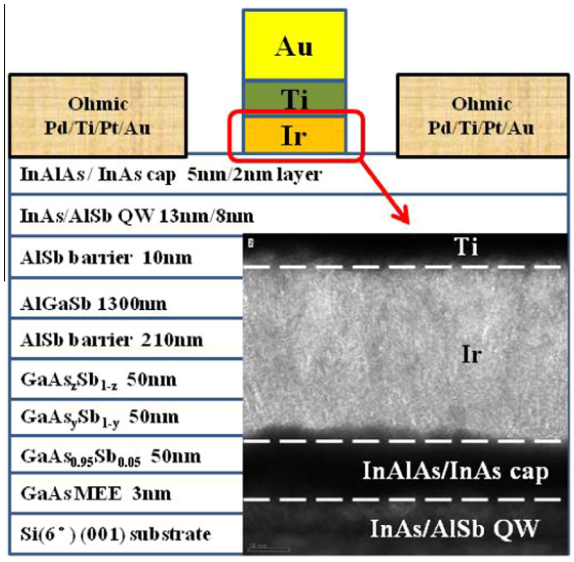

Fig. 2. The HEMT structure and TEM image under the gate electrode.

was used to reduce the ohmic contact resistance. This InAs/AlSb HEMT demonstrated a sheet charge density of 3×10^{12} cm^{-2} together with a Hall mobility of 10,500 cm^2/V-s at 300 K [7]. The energy band diagram of InAs/AlSb on silicon substrate was shown is Fig. 1. Owing to the wide bandgap characteristics of AlSb/AlGaSb/AlSb composited back barrier layer. The InAs 2DEG achieved the good carrier confinement and carrier mobility.

Devices were processed by conventional optical lithography and a lift-off process. The ohmic contacts were realized using Pd/Ti/Pt/Au (20 nm/40 nm/40 nm/50 nm) alloy followed by a 300 °C, 10 s RTA annealing in N_2-rich ambient. To define an active region, the BCl_3 gas was used for dry etching by a reactive ion etching (RIE) system, with a mesa depth of 100 nm. An Ir/Ti/Au (10 nm/20 nm/300 nm) composited gate metal was deposited by electron-beam evaporator for gate electrodes. Then a 300 nm Ti/Au was deposited for interconnection and probe pads. Finally, a 300 nm SiN_x was deposited using plasma enhanced chemical vapor deposition (PECVD) chamber at 200 °C for the device passivation layer. As to the device layer geometry for on-wafer characterization, the 1 μm gate length located in the center position of a 5 μm drain–source spacing and the device transmission electron microscopy (TEM) image was shown in Fig. 2.

3. Device measurements and analysis

The cryogenic DC and low frequency noise system uses coplanar waveguide probes in a vacuum station (JANIS ST 500) to reduce the

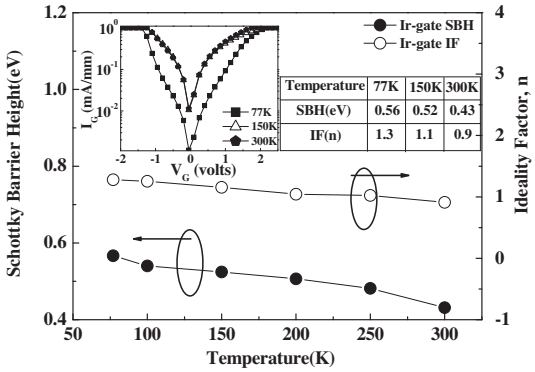

Fig. 3. The device Schottky barrier height and ideality factor characteristics of Ir-gate HEMT from 77 K to 300 K operation.

environment interference for high precision measurement. The current–voltage characteristics of the Schottky gate of Ir-gate AlSb/InAs HEMT were shown in Fig. 3 from 77 K to 300 K. Also shown in Fig. 3, a very low gate leakage current density (I_G) on the order of 10 μA/mm at 300 K was measured at $V_{GS} = 0$ V. The leakage current level is very close to the leakage current published in the previous AlSb/InAs HEMT on InP substrate [8]. When cooled down the sample to 77 K, the gate current is further reduced one order of magnitude. An obvious shift in forward voltage of the gate Schottky diode of 0.12 V was also observed when cooling down to 77 K. This shift is due to the temperature dependence of the built-in potential of the Schottky diode [9]. Current–voltage (I–V) measurement is the most popular and direct way to determine the Schottky barrier height. The thermionic current–voltage relationship of a Schottky barrier diode is given by

$$I = I_s\left[\exp\left(\frac{qV}{\eta kT} - 1\right)\right] \tag{1}$$

where I_s is the saturation current

$$I_s = AA^*T^2 \exp\left(\frac{-q\Phi_B}{kT}\right) \tag{2}$$

A is the diode area, and A^*, Φ_B, η represents the effective Richardson's constant, the effective barrier height, the ideality factor at the measurement temperature T, respectively. For an ideality Schottky diode $\eta = 1$, I_s can be obtained by an extrapolation of the log(I) versus V (forward bias) curve to $V = 0$ using Eq. (1) and η is determined from its slope. Once I_s is known, the Schottky barrier height can be easily calculated from Eq. (2) and given by [10]:

$$\Phi_B = \eta\frac{kT}{q}\ln\left(\frac{AA^*T^2}{I_s}\right) \tag{3}$$

The Φ_B was extracted from the Eq. (3) as 0.56 eV at 77 K operation and this value was increased to 0.43 eV at 300 K operation because the thermionic-field induced tunneling current can be suppressed at cryogenic temperature operation. In addition, The Ir-gate device can maintain a relatively stable ideality factor from 77 K to 300 K owing to its high Schottky barrier height on Si substrate.

The common-source output characteristics of device under 77 K and 300 K operations were shown in Fig. 4. The drain characteristics feature didn't show an unexpected increase in drain current related to impact ionization owing to this high work function refractory gate metal design. Moreover, the lattice scattering phenomenon was further reduced at 77 K operation for AlSb/InAs HEMTs. It is noted that an obvious saturation behavior was observed for drain current close to V_{DS} = 100–200 mV at 77 K

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