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Using oscillation voltage to drive dynamic-domino circuits for designing low-power bio-implanted electronics

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ABSTRACT

Power supply is a key constraint for designing bio-implanted electronic devices. Most conventional internal bio-electronic systems are expected to produce power through wirelessly transmitted technology. However, due to the low efficiency of wireless transmission, the technology cannot be validated. Current generic static CMOS circuits require a constant-level voltage (DCVdd) supply – otherwise, the circuits will malfunction. This work demonstrates that the oscillation voltage (OscVdd) can be directly applied to low-speed dynamic-domino circuits. We successfully designed a test chip that uses OscVdd (validated by TSMC 0.18 μm technology). Compared to DCVdd, OscVdd chips allow for a 68% reduction of dynamic power consumption. With the latch functionality enabled, the OscVdd chip results in a further 42% reduction of power consumption. Therefore, wireless inductive power can be broadly used for future bio-electronics internal human body medical care applications, which are designed by using dynamic-domino circuits.

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1. Introduction

Power consumption of conventional CMOS circuits contains dynamic and static parts. The general CMOS circuit power model is given by the equation $P \risingdotseq CVdd^2f$, where power consumption is proportional to circuit loading (C), supplied voltage (Vdd), and circuit clock frequency (f). Most of the power consumption is dynamic power consumption, which is caused by raising voltage level and the clock frequency. The circuit's parasitic capacitance continually charges during CMOS circuit switching, causing higher dynamic power consumption.

Bio-implanted electronic devices can be used inside the human body to diagnose human diseases and to transmit the diagnostic results for external observation. An example of a physical application is shown in Fig. 1. Limited volume (size) and low-power consumption are essential requirements for these devices. Currently, in order to maintain the instrument's functionality, bio-implanted electronic devices use an un-chargeable battery that requires replacement after a period of time. With wireless power transmission techniques, the battery can be recharged, and thereby eliminating the unnecessary invasive surgery pain, as well as additional suffering and medical expenses.

Generic bio-implanted electronics require stable electric voltage provided to the static CMOS circuit from a battery. Several researchers [2–6] have proposed applying wireless transmission power, as shown in Fig. 2. The wireless transmission power technique transmits a sinusoid signal to an implanted device. This technique needs a voltage regulator to supply a stable voltage to the CMOS static circuit. The device uses a rectifier and a regulator to transform sinusoid-like variable level voltage (ACVdd) to a constant level voltage (DCVdd) for the device's CMOS circuit. However, the energy usage of this technique continues to be a major issue because too much energy is lost during the transformation from the inductive-coupling power devices, including the rectifier and the DC converter (both of which are part of the transformation mechanism).

The inductive-coupling power supply is not efficient. Therefore, there are limited logic gates that can be driven by using this technique. In addition, the transformation devices occupy a large amount of the die's size.

For these reasons, bio-implanted electronic devices require the periodic replacement of batteries. A commercially-implanted device uses wirelessly powered techniques is largely ineffective currently. Thus, power issues remain a major obstacle to the development of bio-implanted electronic devices.

The function of conventional CMOS static circuits is determined by PMOS-charge and NMOS-discharge operations. The circuit will malfunction if ACVdd is supplied to the CMOS static circuit. This is because ACVdd cannot fit all possible combinations of input patterns to be synchronous with the CMOS transistor charge and

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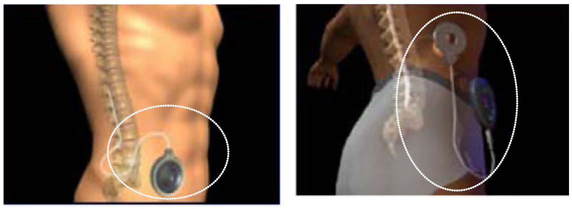

(a) Drug pump (b) Neural stimulator

Fig. 1. Examples of feasible bio-implanted devices.

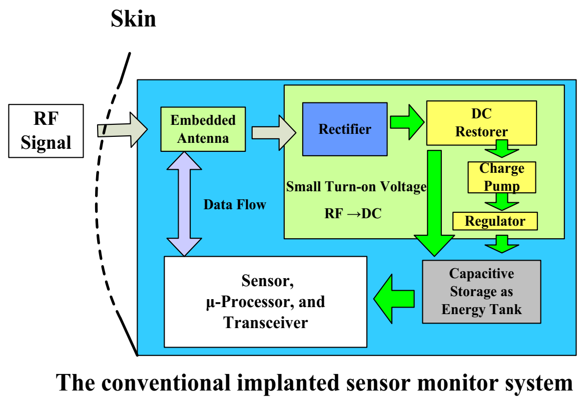

Fig. 2. The conventional coupling transmission bio-system.

discharge operations. The ACVdd needs to be rectified to a stable DCVdd before it is applied to the CMOS static circuit.

The oscillation-type voltage (OscVdd) also cannot be used directly to drive the static CMOS circuit. Furthermore, as the induced current supply to the designed circuit is limited, the voltage transformations from ACVdd and OscVdd to DCVdd are inefficient.

2. Literature review

The AC–DC rectifier and DC–DC voltage converter techniques are the most widely-used in conventional power chip design techniques, as shown in Fig. 3. For the conventional DCVdd design, the power overheads due to the AC–DC rectifier and other associated power transformation circuits (e.g. DC–DC converter) need to be taken into consideration when using static CMOS logic.

The AC–DC rectifier and DC–DC converter are complex because they use many operation amplifiers (OPs) to judge and maintain voltage levels. Each OP supports one specific voltage level comparison. The AC–DC rectifier, DC–DC converter and passive components (discrete inductor, and capacitor) need to be implemented within a power circuit. However, they cannot be integrated within in a single chip. The target design chip isolates the power supply components from other functional blocks in order to minimize the interference within a designed circuit.

Another well-known sinusoidal voltage technique is the Pass-Transistor Adiabatic Logic (PAL) circuit technique [7]. The PAL gates are driven by a two-phase power clock (PC). The PC is a specific sinusoidal type (sinusoid-Vdd) outer power source. This type of power source supply to an adiabatic circuit provides a time-varying, periodic output voltage that gradually swings between 0 V and Vdd. In this PAL adiabatic logic circuit, the ground node is connected to the power supply in order to eliminate the non-adiabatic energy consumption. Fig. 4 shows the PAL inverter cell and a four-stage inverter chain. In contrast to the conventional CMOS circuits, the transition time of the sinusoidal power is long enough to maintain a small potential drop in the transistors. The

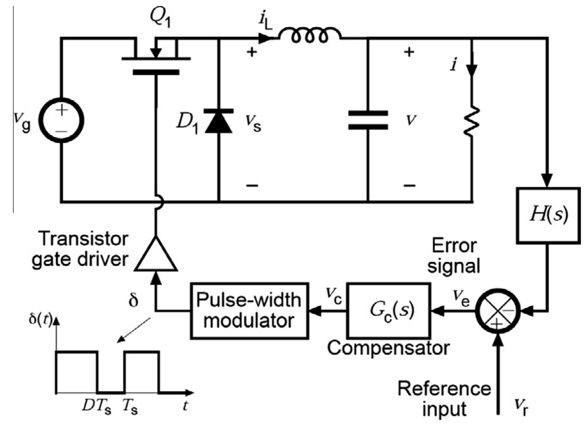

Fig. 3. The DC–DC buck converter circuit structure [11].

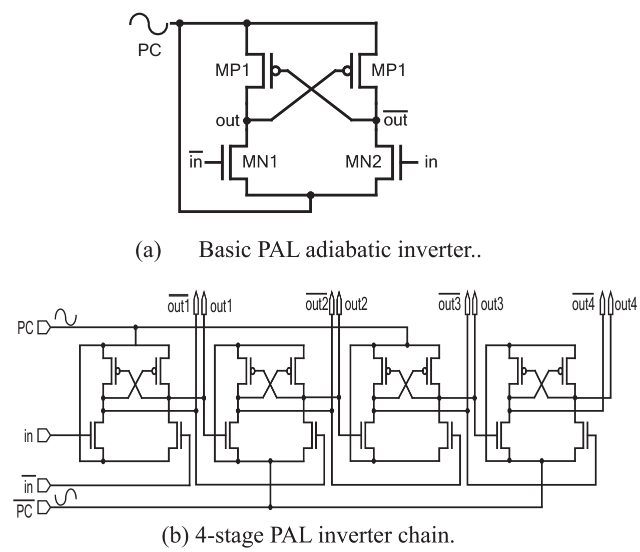

Fig. 4. PAL adiabatic circuit.

adiabatic design minimizes the voltage-drop across the switching devices.

The PAL technique has proven that the use of a slow-rising Vdd can save energy. However, the sinusoid-Vdd of the PAL technique needs specific types of an outer power supply to the circuit.

The PAL technique requires complex control circuits to generate these types of Vdd. They are not suitable for integration with other circuits on a single chip. To the best of our knowledge, only a few empirical studies have been published on the use of PAL techniques [7–10]. Furthermore, pulse-type and sinusoidal-type voltages are impractical for analog circuits. Thus, PAL technique is not popularly used in CMOS circuits.

3. The low-power oscillation voltage dynamic-domino circuit design

3.1. Using oscillation voltage

In this paper, the proposed design technique is designed for internal bio-implanted electronic devices. We propose an OscVdd drive dynamic-domino circuit technique where the OscVdd voltage variances are like a positive-level sinusoid signal. The proposed bio-electronic design uses the inductive coupling technique to transmit OscVdd directly to the dynamic-domino CMOS circuit.

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