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Electrical behavior of the Diamond layout style for MOSFETs in X-rays ionizing radiation environments

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ABSTRACT

This paper aims to describe some innovative layout styles, which are capable to boost the electrical performance and, in the same time, the Total Ionizing Dose (TID) tolerance of Metal-Oxide-Semiconductor (MOS) Field Effect Transistors (MOSFET), without burdening the current planar Complementary MOS (CMOS) Integrated Circuits (ICs) manufacturing processes. To illustrate the potential use of these new alternative devices in analog and digital CMOS ICs applications, this work focuses on the Diamond layout style for MOSFET that presents hexagonal gate geometry. The new effects associated to this innovative transistor structure and its modeling are presented and discussed in detail. Some experimental results are illustrated to evidence its use mainly in space and medical CMOS ICs applications.

1. Introduction

The efforts in research and development (R&D) in Nanoelectronics area are basically grounded in four categories: 1 — *new Complementary Metal-Oxide-Semiconductor (CMOS) Integrated Circuits (ICs) manufacturing processes*: for instance, to manufacture new ICs substrates (Silicon-on-Insulator, SOI [1] and Silicon-on-Sapphire, SOS [2], etc.), new silicon-film for gate region (strained silicon [3], etc.), new gate insulators (high-k, etc) [4], new process to manufacture the three dimensional (3D) chip stack [5], etc.; 2 — *new materials*: copper [6], germanium [7], carbon nanotubes [8], graphene [9], etc.; 3 — *new MOSFETs structures*: considering the planar devices, we have the Ultrathin Buried Oxide (UTBOX) [10], Ultrathin Thin Body SOI (UTB) [11], and regarding the 3D devices, we have the FinFETs [12], Cynthia [13], Pillar Surrounding-Gate [14], Silicon Nano-Wire [15], etc.; and 4 — *the hardness-by-design techniques*: use of the Enclosed Layout Transistors (ELT), for instance, the annular gate shape, edgeless (MOSFET), which are capable to reduce the TID effects [16], implementation of double guard rings around p-wells and n-wells, biased to constant voltages, prevents single-event latch-up (SEL) [17], use of the redundant logic such as the error correcting codes (ECC) [18], etc. However, all these approaches described above involve either a high capital investments or an increase in silicon area of ICs or still an aspect ratio limitation of MOSFETs (by using the ELT structures [16]). But, there is a technique still very little explored by the Semiconductor and ICs Industries, which uses innovative layout styles for MOSFETs, which does not add any extra burden for the current CMOS ICs manufacture processes. This new layout approach is based on the pn junctions engineering between the drain/source-channel regions [19–23]. This new concept can be translated as a simple layout change of the gate geometric shape of MOSFETs, for instance, the hexagonal (Diamond) [19–23], the octagonal (OCTO) [24–27], the Ellipsoidal [28], the FISH (gate geometric shape like the "less than" mathematical symbol, <) [29], and the Wave (gate geometry like an "S" letter) layout styles [30–31]. Besides, new effects give rise as a consequence of changing the MOSFETs layouts result.

Several three-dimension numerical simulations and experimental data studies have been performing with these different layout styles for MOSFETs in room temperature [19–31], in high temperatures [23] and in radiations environment (protons [22] and X-rays [26–27,30–31]). All of these works have been demonstrating that these innovative layout styles are capable to boost the MOSFETs electrical performance and the radiation tolerance [19–31] in analog and digital CMOS ICs applications.

It is known that the key element of direct current (DC)–DC converters is MOSFET switch [32]. By reducing the on-state resistance (R_{ON}) value of the MOSFET switch, it is possible to improve the electrical performance of DC–DC converters [32]. These converters are widely used in electronic space, mainly in satellites and rockets [32].

New effects are amalgamated in the MOSFET structure by using innovative layouts for MOSFETs, such as the Longitudinal Corner Effect (LCE) [19–23], parallel connection of MOSFETs with different channel lengths effect (PAMDLE) [20–23] and deactivation of parasitic MOSFETs in bird beaks regions effect (DEPAMBBRE) [27]. All these effects occur in the same time in Diamond MOSFET structure. The LCE and PAMDLE are

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responsible to boost the analog and digital electrical performances and DEMPAMBBRE is able to improve the ionizing radiation tolerance of the MOSFETs [27].

A previous ionizing radiation study with the Diamond MOSFET was performed in protons radiation environment. The experimental results have demonstrated that the hexagonal gate shape can be considered as optional hardness-by-design technique in order to boost the MOSFET radiation tolerance [22].

In this context, the objective to this manuscript is to investigate the impact of using the Diamond layout style for MOSFETs in the X-rays radiation environment focusing in digital CMOS ICs applications, mainly for DC–DC converters.

2. The innovative hexagonal gate geometry (Diamond) for MOSFETs

In this section the main constructive and electrical features of the Diamond MOSFET (DM) and its electrical behavior under radiative environment are presented.

2.1. Motivation of its creation

Knowing that the MOSFET drain current (I_{DS}) is directly proportional to the longitudinal electric field (LEF), due to the drain bias (V_{DS}), the Diamond layout style was specially designed to use the Corner Effect (CE) present in the three-gate MOSFETs [1]. However, now the CE is applied in the longitudinal direction of the MOSFET channel regarding any planar CMOS ICs technologies. This effect was named Longitudinal Corner Effect (LCE) [19–23]. Thus, when a hexagonal gate geometry is defined to a MOSFET, two LEF vector components ($\overrightarrow{\varepsilon_1}$ and $\overrightarrow{\varepsilon_2}$) are created perpendicularly to the pn junctions between the drain/channel region/source region, due to the V_{DS} and consequently the DM LEF vector resultant ($\overrightarrow{\varepsilon_{//}} = \overrightarrow{\varepsilon_1} + \overrightarrow{\varepsilon_2}$) is higher than the one observed in the conventional (rectangular gate geometry) MOSFET (CM) counterpart, which presents only one LEF vector component ($\overrightarrow{\varepsilon_1}$), regarding the same gate area (A_G), channel width (W) and bias conditions [19], accordingly Fig. 1. Therefore LCE effect is capable to boost the DM LEF and consequently to boost the DM I_{DS} too, in comparison to the I_{DS} of its corresponding CM counterpart, regarding the same A_G, W and bias conditions [19–23].

In Fig. 1, the b and B are the smallest and highest channel lengths of the DM hexagonal gate region, respectively, the W is the channel width and the α is the angle between the metallurgical pn junctions of the source/silicon-film (channel region) and the silicon-film/drain regions of the DM.

To implement two MOSFETs with the same gate areas (A_G), where one is the DM and the other is the CM, it is necessary that the CM channel length (L) equals (b + B)/2 [21–23].

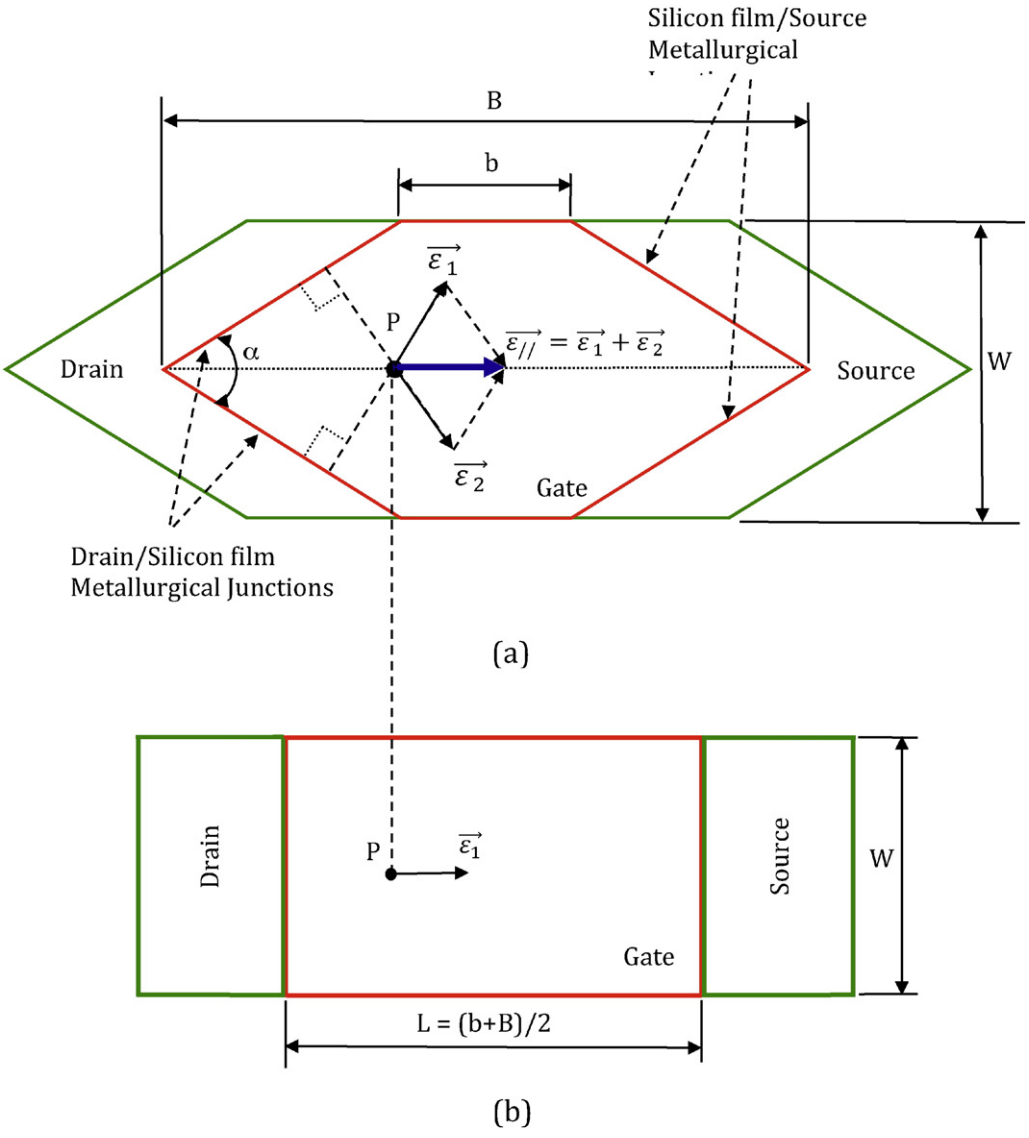

Fig. 1. The simplified top views of the Diamond (a) and its Conventional counterpart (b), regarding the same gate area, W and its corresponding LEF vector components.