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Fabrication and characterisation of suspended narrow silicon nanowire channels for low-power nano-electro-mechanical (NEM) switch applications

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ABSTRACT

Suspended silicon nanowires with narrow (~10 nm) conduction channel are fabricated and characterised for further development of low power nano-electro-mechanical (NEM) switching devices using CMOS compatible fabrication. Double suspension fabrication process using an amorphous silicon sacrificial layer and xenon difluoride etching is employed for thermally-oxidised suspended Si nanowire channels. Device current–voltage characteristics demonstrate depletion mode operation of heavy doped nanowires with an on/off ratio of 10^5 and a threshold voltage of −1.8 V. In plane electromechanical pull-in to side gate is demonstrated and confirmed to be consistent with finite element analysis.

1. Introduction

Leakage current in complementary metal–oxide-semiconductor (CMOS) technology below the 45 nm feature scale is expected to lead to increased power dissipation. To maintain previous performance increase rates, metal–oxide-semiconductor field effect transistor (MOSFET) technology scaling is still continuing. Due to increased power dissipation, MOSFET fabrication is driving towards innovations in materials and new device structures for logic circuits [1].

Nano-electro-mechanical systems (NEMS) are considered as potential candidates for low power switch integration due to the possibility for steep subthreshold slopes [2] and near zero leakage currents [3]. Existing NEMS designs include graphene [4,5,6], carbon nanotubes [7], silicon carbide [8], silicon [9] and metal [10,11]. Additionally, the possibility of exploiting the stored mechanical energy has been proposed for creating two stable state switches [12,13]. Progress of contact NEMS switches and the relationship of the stiction force and the electromechanical forces are detailed in [14]. Other competing technology solutions include magnetic coupled spin-torque devices [15,16], resistive random access memory (ReRAM) [17], phase change memory (PCM) [18], magnetic tunnel junction devices (MTJs) [19,20]. However, these candidates potentially come with complex fabrication, exotic material requirements and CMOS fabrication compatibility issues.

The motivation of this work is the design and fabrication of non-volatile bistable low power sleep transistors for advanced power management in logic circuits. This paper describes fabrication and characterisation of suspended silicon nanowire devices previously reported in [21]. The aim is to create a bistable non-volatile NEMS switch which exploits stiction upon mechanical contact with either side gate electrode. Two potential switching mechanisms are considered for these devices: (i) direct electrical contact from gate to drain; (ii) depletion induced in the nanowire by opposite doping profile at *one* gate electrode, requiring insulated surfaces during mechanical contact.

Electrostatic current modulation is observed in a suspended conducting channel with heavy doping and consequent linear current–voltage characteristics. The fabricated devices exhibit excellent electrical isolation from two opposing side gate electrodes. Measured electro-mechanical pull-in conforms to expected results verified by finite element method simulation. Device destruction is observed after lateral electromechanical pull-in due to the high pull-in voltage required for the prototype doubly clamped beam design. This result is compared with results of devices fabricated

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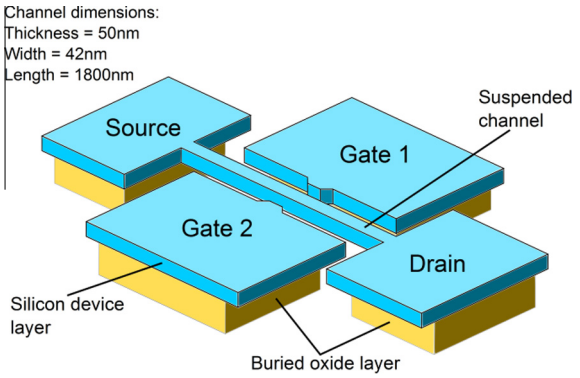

Fig. 1. Schematic diagram of suspended silicon nanowire configuration [21]. The suspended nanowire conducting channel is 1800 nm in length with a 42 by 50 nm cross section. Two opposing side gates, separated by a ~50 nm air gap, are used to electrostatically actuate on and off current conditions.

using lightly doped silicon which avoid the joule heating induced beam destruction observed in the heavily doped devices.

The suspended silicon nanowire device configuration presented here consists of an oxidised silicon channel with a 42 nm by 50 nm total cross section and length of 1800 nm. Source and drain electrodes are at either end of the suspended channel, which is flanked by two opposing side gates with a separating air gap of ~50 nm. This is illustrated in Fig. 1.

2. Fabrication

Suspended silicon nanowire devices are fabricated on ultrathin silicon-on-insulator (SOI) substrates with a device layer thickness of ~50 nm. The device layer is phosphorus doped to a concentration of $\sim 1 \times 10^{19}\ cm^{-3}$ using spin-on phosphorosilica film (2500 RPM for 60 s) followed by annealing at 925 °C for 8 min.

Nanoscale device features are patterned by electron beam lithography using a JEOL 9300 JBX Electron Beam Lithography System. Ebeam exposure of 29 nm hydrogen silsesquioxane (HSQ) realises channel widths of around 42 nm on 50 nm thickness SOI. Smallest features are patterned with a fixed dose of 1750 $\mu C/cm^2$ at 1 nA beam current, 5 nm spot size and shot pitch of 4 nm. To reduce ebeam exposure times, large features are patterned during a second exposure using a 10 nA beam current, 24 nm spot size, 20 nm pitch and process error correction with on-chip global alignment marks.

An Oxford Instruments capacitive reactive ion etching (RIE) tool is used to etch device features using sulphur hexafluoride (SF_6) and oxygen (O_2) chemistry. Both gases are introduced to the chamber at a constant rate of 36 sccm, RF power is maintained at 100 W. This results in vertical sidewalls and an etch rate of around 1.5 nm/s.

The silicon nanowire channel is suspended using hydrofluoric (HF) acid under-etching of the 200 nm thick buried oxide (BOX) layer using an Idonus HF vapour phase etcher. HF etch is performed at 45 °C. The resultant etch of the BOX layer is variable, 5 min exposure cycles etch between 30 nm and 60 nm, ellipsometry and SEM imaging are used to monitor the etch progress between etch cycles. Vapour phase etching eliminates capillary force induced stiction to the substrate which is observed when under-etching using liquid etchant [22]. After the first suspension stage a thin oxide layer is thermally grown on the surface of both side gates and the suspended nanowire at 825 °C for 12 min under an O_2 flow of 5 slm (Fig. 2(a)). This process is used to passivate the silicon nanowire and to create an insulating layer.

A ~600 nm thick sacrificial layer of amorphous silicon (a-Si) is then deposited by plasma enhanced chemical vapour deposition (PECVD) to protect the suspended silicon nanowire channel during metallisation (Fig. 2(b)). The sacrificial a-Si layer is fabricated using an Oxford Instruments PlasmaLab System 100. The system uses capacitively coupled RF plasma at 13.56 MHz to disassociate source gases silane (SiH_4) and hydrogen (H_2) for deposition onto a heated substrate (250 °C). 50 sccm SiH_4 and 50 sccm H_2 flow

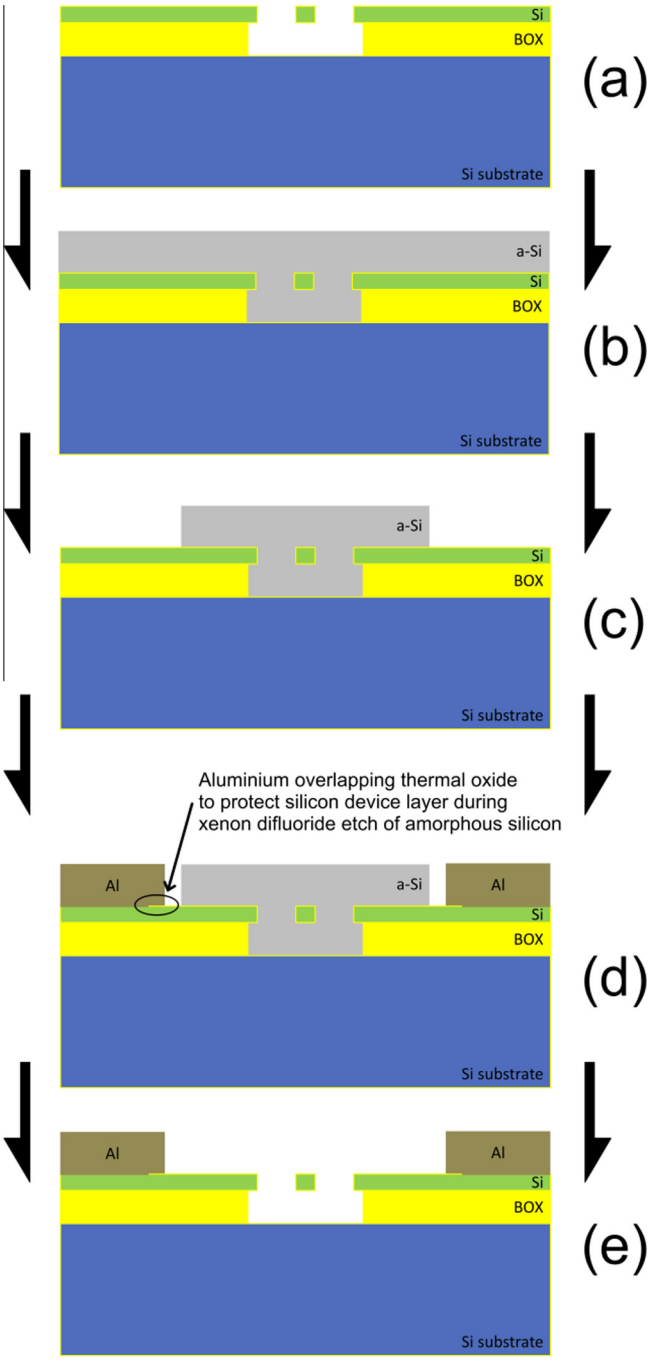

Fig. 2. Cross section illustrations of the critical stages of fabrication for the suspended oxidised silicon nanowires. (a) After suspending the nanowire by vapour HF and thermal oxide growth, (b) low rate deposition of the amorphous silicon sacrificial layer is critical in order to ensure the suspended nanowire is not damaged and that a high-density protective film is achieved. (c) Patterns of varying sizes are prepared before metallisation using AZ2070 photoresist to etch through the a-Si and the thermal oxide layers. (d) By design, aluminium contact pads overlap the thermal oxide layer to protect the underlying silicon device layer during the final a-Si etching step. (e) Final XeF_2 vapour release stage etches sacrificial a-Si but not the 50 nm silicon device layer because of the thin thermal oxide surface.