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Flexible silicon nanowire low-power ring oscillator featuring one-volt operation

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ABSTRACT

In this study, we propose a flexible silicon nanowire (SiNW) low-power ring oscillator, which features 1-V operation. Our flexible ring oscillator is composed of three CMOS inverters with a gain of 70 at a supply voltage of 1 V. *p*- and *n*-channel SiNW field-effect transistors (FETs) forming the component inverters exhibit on/off current ratios of 4.36×10^4 and 1.46×10^5, respectively. Our ring oscillator generates a sinusoidal wave with a frequency of ~6.6 MHz. The frequency and waveform are undistorted under upwardly bent and downwardly bent strain conditions of 0.7%. The good mechanical bendability of the flexible ring oscillator indicates high stability and good fatigue properties.

1. Introduction

Flexible electronics is an emerging field of technology because of their applications in portable consumer products. Among active materials used in flexible electronics, one-dimensional (1-D) materials such as nanowires (NWs), carbon nanotubes (CNTs), and graphenes have been studied widely because of their superior electrical characteristics such as 1-D ballistic transport, which reduces the transverse energy component. Moreover, their three-dimensional (3-D) gate structures enable more effective control of the flow of charge carriers in channels, relative to planar bulk-based FETs [1–4]. Particularly, silicon nanowires (SiNWs) offer an appealing approach because of the well-established knowledge of Si and their process compatibility with existing Si-based technologies [5–7].

Power consumption is an important consideration in flexible electronics, as circuits follow the continued dimensional and functional scaling trend [8–11]. One approach to extending flexible technology is to replace devices with complementary metal–oxide-semiconductor (CMOS) technology. CMOS circuits have advantages over individual *n*- or *p*-channel devices because they combine both *n*- and *p*-channel FETs. In CMOS circuit operation, one of the *n*- and *p*-channel FETs is always turned off when the other turns on in logic states. Therefore, the power consumption of CMOS circuits is relatively low. The other approach is to reduce the supply voltage, which is a common method for achieving low power consumption in integrated circuits. The reduction of power has become a critical issue as device performance is increased. Nevertheless, there are complex tradeoffs in the optimization of device performance while reducing supply voltage, posing significant circuit design challenges [12]. Currently, most devices based on low-dimension materials operate at a relatively high supply voltage [13–16]. In this study, we investigate the dynamic electrical characteristics and reliability of a SiNW-based flexible ring oscillator on a plastic substrate that is capable of operating at a supply voltage of 1 V, achieving low power consumption and stable performance.

2. Material and methods

2.1. SiNW fabrication

The SiNWs were derived from a *p*-type bulk silicon wafer doped to $\sim 1 \times 10^{16}$ cm^{-3} using a fully CMOS-compatible top-down route. As shown in Fig. 1a, a Si trench was fabricated on a bulk Si wafer using anisotropic dry etching. The Si trench was selectively wet etched in tetramethyl ammonium hydroxide (TMAH, $(CH_3)_4NOH$; 25%, diluted in water) solution to form the inverted triangular SiNWs, as shown in Fig. 1b. The size of the SiNWs was reduced using thermal oxidation. The source/drain regions of the SiNWs were heavily doped using separate masked ion-implantation with As^+ (*n*-type dopant) and BF_2^+ (*p*-type dopant) ions at a dose of 5×10^{15} cm^{-2} and ion energies of 80 and 50 keV, respectively. Finally, the wafer was annealed at 900 °C for 60 min in a nitrogen ambient and at 1000 °C for 10 s both to activate the implanted dopants with uniform diffusion and to eliminate defects. The

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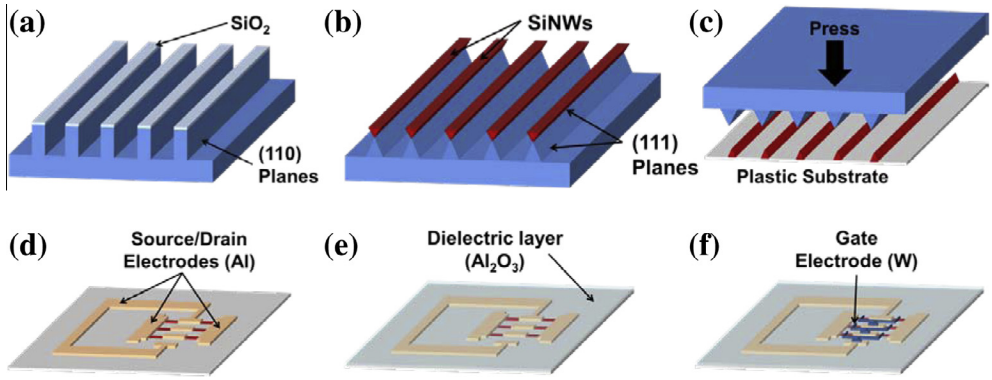

Fig. 1. SiNWs and device fabrication for flexible ring oscillator on a plastic substrate. (a) Si-trench fabrication on a bulk Si wafer through anisotropic dry etching. (b) Wet etching with TMAH solution and forming inverted triangular SiNWs. (c) Direct transfer of triangular SiNW arrays onto plastic substrate. (d) Formation of source/drain electrodes using photolithography and thermal evaporation. (e) Formation of a dielectric layer (Al_2O_3) using atomic layer deposition. (f) Formation of gate electrodes (W) using DC magnetron sputtering.

surrounding oxide was then removed using a buffered oxide etch (BOE) solution to release the SiNWs from the Si substrate [17–19].

2.2. Ring oscillator fabrication

A flexible ring oscillator was fabricated on a polyethersulphone (PES; 200 μm thick) plastic substrate by transferring the as-fabricated SiNWs (~100 nm diameter) from the Si wafer shown in Fig. 1c [17–19]. Our 3-stage ring oscillator is composed of three CMOS inverters, which are combined with pairs of *n*- and *p*-type SiNWs. Shown in Fig. 1d–f, source/drain aluminum metal electrodes (~100 nm) were formed by photolithography and then deposited using a thermal evaporation process. Next, high-*k* Al_2O_3 gate dielectric layers (~25 nm) were formed using the atomic layer deposition (ALD) technique at 150 °C. The vias between source/drain and gate metal electrode layers were formed using photolithography and a BOE wet etching process to connect all of the CMOS inverters in a loop. Finally, the tungsten top-gate electrode layers (~150 nm) were fabricated using photolithography followed by DC magnetron sputtering.

2.3. Electrical measurements

The electrical characteristics of the ring oscillator were investigated using a semiconductor parameter analyzer (HP 4155C) at room temperature in air. AC input signals were generated by a function generator (Agilent 81150A), and the frequency characteristics of the ring oscillator were examined using an oscilloscope (Agilent MSO7052B). Bending tests were conducted with a custom-built bending machine.

3. Results and discussion

Our 3-stage ring oscillator is composed of SiNW-based CMOS inverters on a flexible substrate. These inverters are connected as a circular chain consisting of pairs of *n*- and *p*-SiNW FETs, as shown in Fig. 2a. Because the output and input electrodes between the inverters are connected directly, the output signal generated by a prior inverter act as the input signal for the next inverter. Fig. 2b is the schematic circuit diagram of the 3-stage ring oscillator.

First, we investigate the electrical characteristics of individual FETs and component inverters of the ring oscillator. Fig. 3a shows the drain current (I_D) measured as a function of the gate-to-source voltage (V_{GS}) of representative *n*- and *p*-SiNW FETs at a drain-to-source voltage (V_{DS}) of ±1 V, respectively. The *n*- and *p*-SiNW FETs forming the component inverters exhibit on/off current ratios of 1.46×10^5 and 4.36×10^4, respectively. The threshold voltages (V_{th}), obtained using the maximum transconductance (g_m) extrapolation method, are 2.52 V for the *n*-SiNW FET and −3.84 V for the *p*-SiNW FET. The point subthreshold swings (SS_{point}), defined as the gate voltage change required to reduce the subthreshold current by one decade, are found to be 118 mV dec^{-1} at V_{GS} = 0.35 V for the *n*-SiNW FET and 273 mV dec^{-1} at V_{GS} = −1.13 V for the *p*-SiNW FET. The static electrical characteristics of a representative inverter are shown in Fig. 3b. The inverter exhibits excellent static transfer characteristics, with a narrow transition width of ~0.35 V and a maximum voltage gain of 70 at a supply voltage (V_{DD}) of 1 V. With these static characteristics, our devices are competitive with other 1-D based inverters using SiNWs (with a gain value of 40 at 1.2 V) [20], ZnO-NWs (with a gain value of 12 at 2 V) [21], single-walled CNTs (with a gain value of 45 at 2 V) [22], or InAs/GaSb NWs (with a gain value of 10.5 at 0.5 V) [23]; our inverters have superior performance at low supply voltages. Additionally, the relatively higher electric field could be formed in the sharp corners of the triangular-shaped SiNW channels (compared to SiNW channels with circular shape), but the formation of the field does not lead to the failure of the reliability of the performance of inverters, especially, for SiNW channels with diameters larger than 10 nm [24–26].

Next, we analyze the AC dynamic characteristics of a representative inverter. The change in the output waveform as a function of the input frequency at a supply voltage of 1 V is measured, as shown in Fig. 4. The output waveforms become distorted as the input signal frequency increases from 100 kHz to 5 MHz. The delay time associated with the charging/discharging times of the load capacitance affects the distortion of the rectangular output waveform. The delay times are dependent on the electrical switching performance of the inverter. Typically, the propagation delay time is acquired by calculating the required time to change from 10% to 90% of the final output level for a low-to-high transition, and from 90% to 10% of the final output level for a high-to-low transition [27]. When the input signal frequency is 5 MHz, the propagation delay times for the low-to-high transition (tPLH) and the high-to-low transition (tPHL) are 6 and 56 ns, respectively. The difference in the delay times results from the characteristic variation of each SiNW and the misalignment between the gate and the channel of FETs, which creates a gate-to-source parasitic capacitance. Thus, the output waveform is distorted asymmetrically, because of the difference in the gate-to-source parasitic capacitances of the *n*- and *p*-SiNW FETs.

Finally, we demonstrate the oscillation characteristics of the flexible ring oscillator. Fig. 5 shows the waveform of the flexible