Microelectronic Engineering 145 (2015) 149–152

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Graphene field effect devices operating in differential circuit configuration

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ARTICLE INFO

Article history:
Received 24 October 2014
Received in revised form 6 February 2015
Accepted 9 March 2015
Available online 28 March 2015

Keywords:
Graphene
FET
Differential signaling

ABSTRACT

We study the concept of a basic building block for circuits using differential signaling and being based on graphene field effect devices. We fabricated a number of top-gated graphene FETs using commercially available graphene and employing electron beam lithography along with other semiconductor manufacturing processes. These devices were then systematically measured in an automated setup and their DC characteristics analyzed in terms of a simple but effective analytical model. This model together with the collected data allowed us to proceed further with both mathematical analysis of circuit characteristics as well as numerical simulation in a dedicated circuit analysis software.

1. Introduction

After decades of miniaturization and performance tuning, silicon electronics is approaching its technological limits [1]. In the search for alternative transistor channel materials, graphene has been given much attention since its discovery in 2004 [2], mainly because it offers compelling values of carrier mobility and a consequent potential for high frequency operation, possibly reaching into the THz range [3]. Certain drawbacks however, such as the weak or absent current saturation or the high "off" current, limit the use of graphene for traditional CMOS-like circuitry [4]. Elementary circuits based on graphene devices, such as an audio voltage amplifier [5] or a logic inverter [6] have already been published. They rely, however, on CMOS-like principles to operate, whereas in this work we investigate the possibility of employing graphene devices for an alternative approach based on differential signaling, where saturation and off-current are not expected to preponderate.

2. Device fabrication

We used samples of commercially available, CVD-grown single layer graphene, transferred onto a silicon substrate covered by 285 nm of SiO_2 (Fig. 1). Channel regions were defined by removing graphene in the surrounding areas by an ion-beam etch. Cr/Au source and drain (S/D) contacts were evaporated and patterned by electron beam lithography (EBL) and lift-off, followed by atomic layer deposition (ALD) of a 15 nm thick Al_2O_3 gate dielectric. Finally, the gate electrode is patterned and deposited similarly to the S/D electrodes. The gate dielectric, which also covers the S/D metal prevents a short circuit with the gate electrode and allows for tight alignment, reducing the length of un-gated channel regions to a minimum. An example of fabricated graphene FET (GFET) is shown in Fig. 2.

3. Characterization and data analysis

Electrical measurements were taken to assess the transistor's DC characteristic. An automated setup was used to apply identical measurement conditions to a large quantity of devices. The resulting drain current vs gate voltage $I_D(V_G)$ and drain current vs drain voltage $I_D(V_D)$ curves were analyzed in terms of several key parameters, using the following expressions for fitting:

$$G_{ds} = \sqrt{g_m'^2(V_G - V_0) + g_0^2}, \quad (1)$$

where G_{ds} is the transistor's overall conductance between source and drain, g_m' is the transconductance per unit of drain-source bias ($g_m' = g_m/V_{ds}$), V_0 is the Dirac voltage, and g_0 is the conductance minimum at the Dirac point ($G_{ds}(V_G = V_0) = g_0$). For simplicity g_m' and g_0 will be referred to as reduced transconductance and base conductance respectively throughout this paper.

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http://dx.doi.org/10.1016/j.mee.2015.03.012
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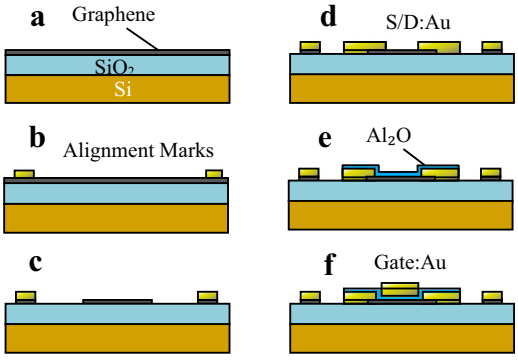

Fig. 1. Fabrication process flow. (a) Substrate Si, 512 μm + SiO_2, 285 nm + graphene (b) alignment marks, Cr/Au (c) graphene etch (d) S/D contacts, Cr/Au (e) gate dielectric, Al_2O_3; (f) gate metal.

This intrinsic conductance translates into an extrinsic output current, when taking the contact resistances into account ($R_S = 2R_C$):

$$I_{extr} = V_{DS}\frac{G_{ds}}{1 + R_S G_{ds}}. \tag{2}$$

These are responsible for the concave bending and eventual saturation of the $I_D(V_D)$ curve far away from the Dirac point. No other current saturation effects, such as carrier velocity saturation due to scattering mechanisms (MOSFET-like pinch off does not exist in gapless single layer Graphene [7]), are taken into account here.

This simple model, albeit empirical rather than based on physics principles, provides excellent fitting results and allows extracting parameters that reflect the device's extrinsic performance relevant for circuit simulation. Similar models, also containing square-root based expressions but tailored to extract physical rather than circuit-relevant parameters were used in the past, e.g. by Meric [8,9] and Scott [10]. It may also be more suitable for hand calculations in the analysis of elementary circuits than complex physical models. Combining a series of $I_D(V_G)$ curves, measured at different drain bias values, and performing a surface fit allows capturing the complete DC characteristic of a device. Surface fits obtained in this manner exhibit a slightly larger residual error compared to individual curve fit but are still acceptable for our purpose (Fig. 3).

4. Differential circuit modeling

The working principle of the differential pair circuit relies on a constant current source in the stem and two switching devices

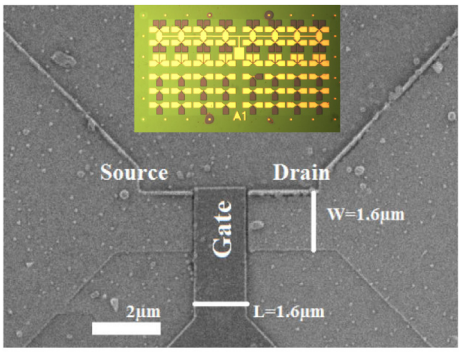

Fig. 2. SEM image of a single graphene FET, with L = 1.6 μm and W = 1.6 μm (to protect the graphene from electron irradiation device was imaged after electrical characterization – hence the contamination). Inset: microscope image of an array of devices, one of 12 per die.

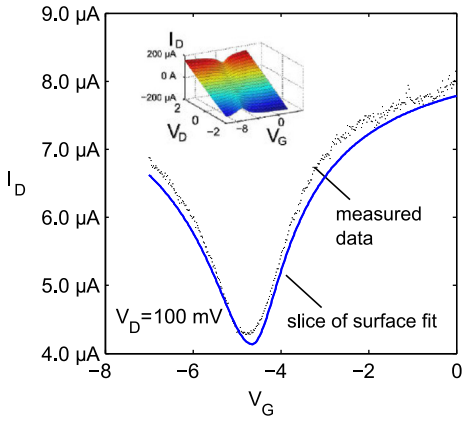

Fig. 3. Typical $I_D(V_D)$ curve. The fit is obtained from multiple $I_D(V_G)$ measurements on the same device with varying V_D. Inset: extrapolation of complete current–voltage characteristic.

directing the current in either one or the other of two "branches" (Fig. 4). The sum of the currents of both branches is therefore constant. The switching effect can be described by an imbalance factor α:

$$\alpha = \frac{I_1 - I_2}{I_S} \tag{3}$$

where $I_S = I_1 + I_2$ is the stem current supplied by the constant current source. In this formulation, the branch currents become

$$I_{1,2} = \frac{1}{2}(1 \pm \alpha)\cdot I_S \tag{4}$$

The output voltage is the difference of the drain nodes in either branch of the circuit:

$$V_{D1,2} = V_{DD} - R_L I_{1,2} \tag{5}$$

$$V_{out} = V_{D1} - V_{D2} = R_L(I_2 - I_1) = -\alpha R_L I_S \tag{6}$$

If we model the graphene devices as conductances G_1 and G_2 (which are each a function of the devices' bias conditions, i.e. V_G) then the total resistance of each branch can be expressed as

$$R_{br,i} = R_L + 1/G_i. \tag{7}$$

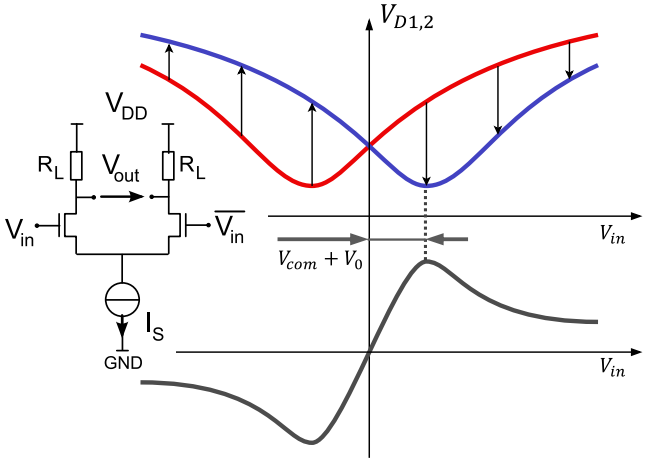

Fig. 4. Circuit schematic (inset) and simplified working principle of the graphene differential pair. Upper axis: left (red) and right (blue) transistor output (drain) voltage, V_D. Lower axis: transfer curve, V_{out}, determined by subtraction of blue curve from red curve. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)