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Optimization of through silicon via for three-dimensional integration

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ABSTRACT

Three-dimensional integration has drawn more and more attention in electronics industry due to its potential of reducing the interconnect delay, improving the device performance and realizing heterogeneous integration, where through silicon via has become the mainstream. In this paper, the key technologies including via fabrication and copper via filling in the through silicon via process were investigated and optimized. We analyzed the micrograss on the via sidewall that would create sidewall profile issues, and modified the etch/passivation recipe to eliminate the micrograss. Vacuuming before electroplating to enhance the wettability of the through silicon via with copper electrolyte was introduced. Magnetic stirring was performed and an improved two-step electroplating process was applied during electroplating. With these optimized processes, we demonstrated defect-free copper filled through silicon vias with shorter plating time and thinner copper overburden on the wafer surface, which is beneficial to the realization of three-dimensional integration.

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1. Introduction

With the rapid trend of semiconductor devices towards high density, high performance, small form factor, low power consumption and low cost in electronics industry, there has been a deviation in continuing the evolution of the Moore's law. Today the three-dimensional (3D) integration technology is widely accepted as an effective approach to maintain the progress in cost and performance for electronics. It enables continuous increase in functional diversification and decrease in cost per function, and allows the scaling in the third dimension. The chip stack packaging based on through silicon via (TSV) can provide the shortest vertical connection path and realize more complicated multichip system integration, which is expected to be a critical technology for realizing 3D integration schemes [1–4].

Key technologies involved in the TSV process include (a) silicon via formation with controlled profile, (b) insulation layer, barrier layer and seed layer deposition with good conformality, and (c) defect-free via filling [5–7]. Deep reactive ion etching (DRIE) based on the Bosch method is usually used to fabricate the silicon vias [8]. This is a time-multiplexed alternating process that alternates etch and passivation steps, each lasting only a few seconds [9]. The etch step, followed by the passivation step, rapidly removes the polymer layer on the bottom of the structure while partially removing the polymer layer on the sidewall. Generally, a vertical or tapered profile with a smooth sidewall is preferred for facilitating continuous insulation, barrier and seed layers deposition [10]. The insulation layer (SiN_x or SiO_2) is deposited by plasma enhanced chemical vapor deposition (PECVD) and the prevalent method for the barrier and seed layers deposition is physical vapor deposition (PVD). The barrier and seed layers must be continuous with good conformality and adhesion to allow the subsequent electroplating for filling the vias. Defect-free filling of high aspect ratio TSVs is a significant process in 3D integration for implementing electrical interconnection of multilayer device stacking in vertical direction. The most common material for via filling is copper, due to its high reliability, high allowed current density, long electromigration lifetimes and low electrical resistance [11,12]. Copper electrochemical deposition (ECD) methods have several characteristics that make them attractive for filling of high aspect ratio vias. These aqueous processes provide super conformal deposition under the correct conditions, and they are more stable for metal deposition. In addition, ECD processes require less costly equipment than vacuum-based processes.

The successful criteria for high aspect ratio TSV electrodeposition are defect free via filling, minimum overburden and reduced deposition time [13]. Though copper electroplating technology for TSV filling has been studied extensively, it is still a challenge to provide void-free filling in TSVs with a high aspect ratio, where incorporated seams or voids in the vias will ultimately cause serious reliability issues [14–16]. Discontinuous seed layer deposition, insufficient wettability of the TSV before plating and uneven distribution of local current density are the major reasons for defects

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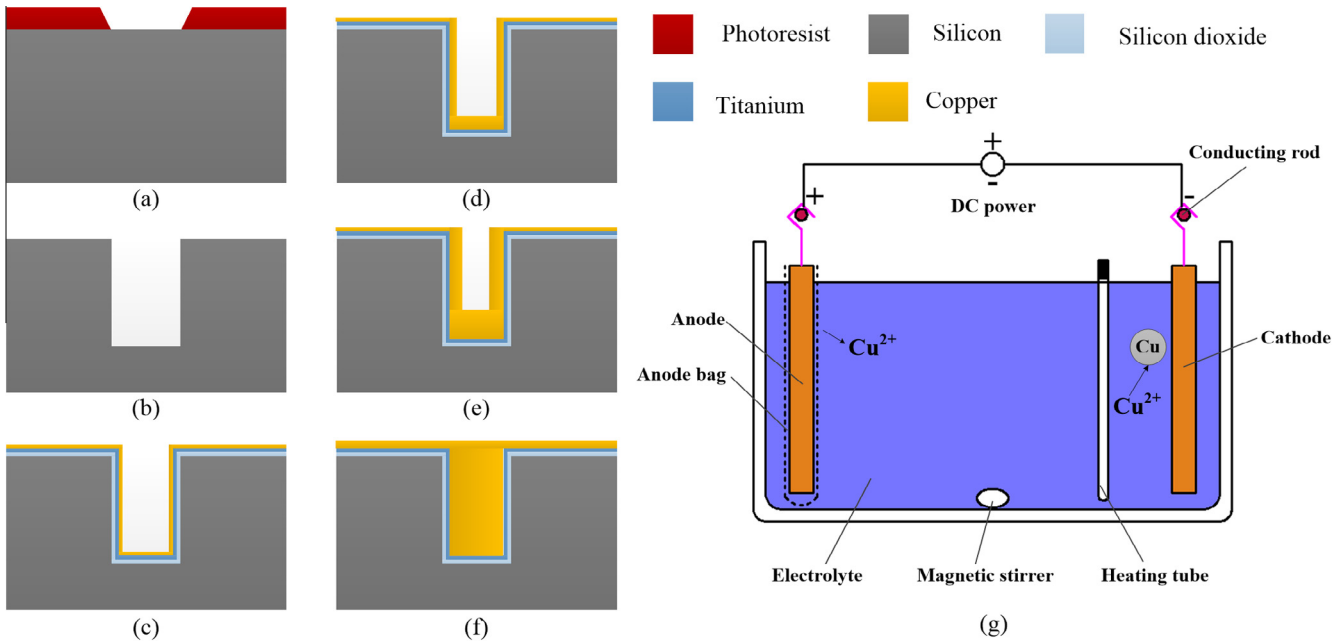

Fig. 1. The super conformal electroplating process together with the copper electroplating system. (a) Patterning photoresist on the wafer. (b) DRIE etching of the vias. (c) Insulation/barrier/seed layers formation. (d)–(f) Super conformal electroplating. (g) The copper electroplating system.

Table 1
DRIE process parameters used for deep etching of TSV.

Process	Main gas	Step length (s)	Flow of SF_6/C_4F_8 (sccm)	P_c/P_p (W)
Etch	SF_6	8	100/5	750/25
Passivation	C_4F_8	10	5/100	750/10

formation [17–19]. Undesired profile of the silicon vias with micro-grass on the sidewall may cause discontinuous coverage of the copper seed layer, which will induce serious defect problems in subsequent copper filling [20,21]. In high aspect ratio silicon via electroplating, the cupric ions at the via entrance transport easier than those at the bottom, and the current crowding effect also leads to faster copper deposition and higher current density at the via top. Thus, the vias are easily blocked at the top, resulting in voids or seams formed inside the vias [22,23].

In this paper, we focused on optimization of the via fabrication and copper via filling in the TSV process, and achieved defect-free copper filled TSVs with shorter plating time and thinner copper overburden on the wafer surface.

2. Experimental procedures

N-type, 4-inch, <1 0 0> crystal orientation silicon wafers with a thickness of 500 μm were used in the experiments. A positive photoresist (PR1-12000A, Futurrex Inc.) with the thickness of 12.8 μm at a coating spin speed of 2500 rpm for 40 s was patterned on the

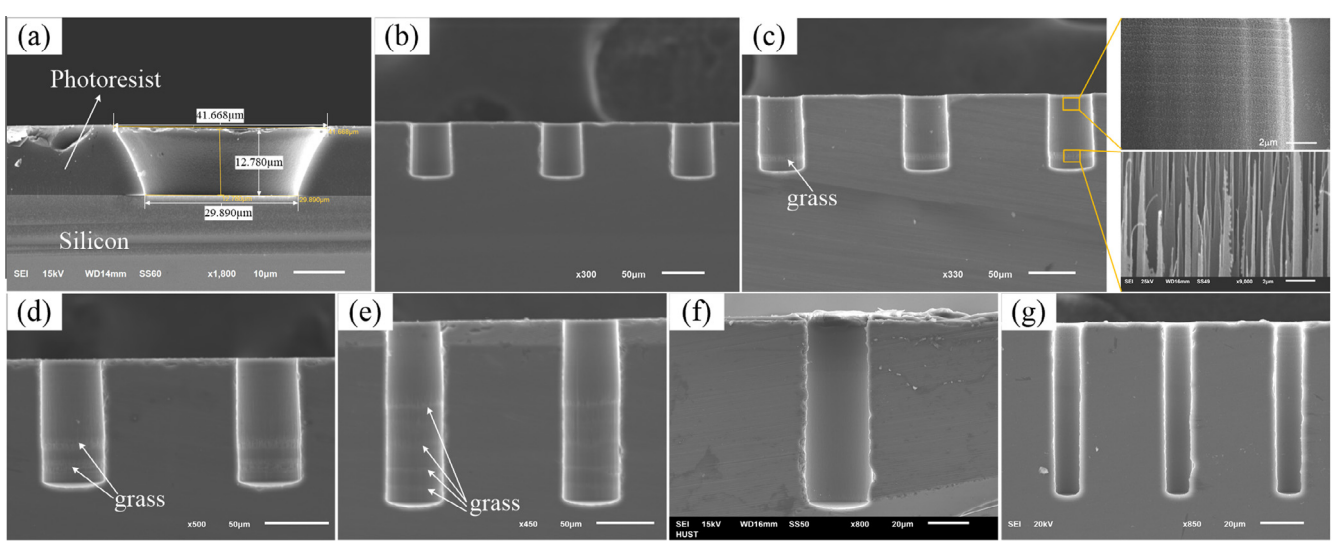

Fig. 2. The profile of the patterned photoresist and the DRIE results of the TSVs. (a) The profile of the patterned photoresist with the via diameter of 30 μm. (b)–(e) TSV samples etched with the etch/passivation recipe of 8 s/10 s, where the diameter is 50 μm and the etch time is 32, 43, 54, 98 min, respectively, and the top magnified image shows the scalloped profile and the bottom magnified image shows the micrograss. (f and g) TSV samples etched with the modified etch/passivation recipe of 8s/5s, where (f) is the TSV with a diameter of 30 μm and an etch time of 43 min, and (g) is the TSV with a diameter of 10 μm and an etch time of 54 min.

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