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Through silicon via profile metrology of Bosch etching process based on spectroscopic reflectometry

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ABSTRACT

Through silicon via (TSV) technology is a key feature of new 3D integration of circuits by creation of interconnections using vias, which go through the silicon wafer. Typically, the highly-selective Bosch Si etch process is used which is characterized by a high etch rate and high aspect ratio forming a series of scallops on the sidewall. The large scallops may reduce the reliability of the devices, appearing as leakage currents, thermo-mechanical stress or slow device response. The etch profile which is defined by top and bottom dimensions, depth, scallop size (period and amplitude) need to be both monitored and well controlled. Usually using secondary electron microscopy (SEM) cross-section image analysis is destructive, time consuming and depends on the cutting technique. In this work, the nondestructive 3D metrology of deeply-etched structures with an aspect ratio of more than 10 and patterns with lateral dimensions from 3 to 7 µm was performed by spectroscopic reflectometry. The TSV depths were determined using the interference effect between waves reflected from TSV's top and bottom surfaces. The scallop size was estimated from the back diffraction effect of light from the side wall. The rigorous coupled wave analysis (RCWA) has been applied for scallop amplitude and top and bottom dimensions evaluation. By the characterization of the scallop size variation, the etch process (etch depth, rate, and reproducibility) can be controlled.

1. Introduction

Through silicon via (TSV) is an advanced technology for stacking silicon devices in three dimensions (3D). Generally, TSVs are formed by etching a vertical via and filling them with a conductive material, such as a copper [1]. TSV technology has opened up new possibilities of 3D integration of micro-electro-mechanical systems (MEMS), photonic circuits, microfluidic devices, or electrical grounding of CMOS and BiCMOS devices [2–4].

Via etching is a critical step in TSV integration impacting isolation, metallization and wafer thinning. Typically, the Bosch process is used to realize a high selectivity, a high etch rate and a high aspect ratio Si dry etching [5]. This process includes repeated alternating isotropic dry etching and sidewall passivation/deposition steps. It creates a series of scallops on the sidewalls in the silicon.

Scallops can be characterized by a depth or amplitude (a), measured as the longest horizontal distance between peaks and side wall, and by period (g), measured as the vertical distance between peaks. Depending on the etching process parameters, the amplitude and period of the scallops can be changed [6]. The scallop amplitude is most affected by the etch cycle time. It decreases greatly along with reduced etch and passivation cycle times. Longer etch cycle times cause a larger scallop period and are responsible for deeper scallops [7].

The scallop period is of secondary importance compared to scallop amplitude when considering the TSV reliability. Large scallop amplitude, for example, may reduce the reliability of MEMS devices, appearing as, e.g., higher leakage currents [8], thermo-mechanical stress [9], or slow device response. So, the leakage current can be diminished by nearly 3 orders of magnitude when the sidewall roughness is minimized or replaced by a smoother sidewall for the top few micrometers using a non-Bosch etch process [8]. By tailoring a short initial etch step to smoothen the top sidewalls, it is possible to minimize the adverse effects of the sidewall scallops.

The etch profile (defined as critical dimensions (CDs) at the top and at the bottom, depth, bottom curvature, scallop size) need to be monitored and well controlled in high aspect ratio TSVs to ensure defect-free coverage of the liner, barrier, and seed thin metal layers.

TSV metrology and inspection, as a new subchapter for 3D Interconnects, was introduced to metrology roadmap [10].

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Usually a destructive cross-sectional scanning electron microscopic (SEM) image analysis is the most frequently used method for the process development and quality control. But SEM evaluation strongly depends on the cutting technique. The sample cut should be prepared in exactly perpendicular direction to the sample surface without misalignment of the position of the cut face from the true center of the via. This issue becomes more significant when via sizes decrease. Moreover, the ability to provide precise control of the TSV etching process at all points on the wafer is extremely important for maintaining a high wafer yield of the devices.

Optical interferometry and reflectometry are the main nondestructive metrological methods for this purpose [11–13] but their use is limited for smaller diameter TSVs due to the requirement of obtaining a measurable signal of reflected light from the bottom of the TSV. The nondestructive 3D metrology of deep-etched structures with an aspect ratio of more than 10 and patterns with lateral dimensions in the range below 5 μm remains a challenge. In our previous paper [13], the inspection of the TSV depth and critical dimensions of their opening was performed nondestructively by an industrial thickness measurement tool (UV-VIS spectral reflectometer). It was shown that spectral reflectometry can be used for the monitoring of geometrical parameters of TSVs with dimensions starting at 3 μm and aspect ratios up to 17:1. TSV profile in high aspect ratio vias is a great inline metrology challenge for 3D integration. In the current paper we have extended the inspection method of the TSV profile by the scallop evaluation. Here, the scallop size (period and amplitude) determination will be presented. In this way, the full control of TSV profile, i.e., the depth, CD of their opening and the dimension of sidewall scallops can be realized by spectroscopic reflectometry.

2. Experimental

The high density TSV arrays consisted of high aspect-ratio square vias with a tapered profile in p-type (Boron) doped Czochralski (CZ) Si (100) with a resistivity of 9–18 Ω cm and a nominal width or CD from 3 to 7 μm, a pitch in the range of 7–11 μm, and etch depths of 50–70 μm were investigated (Table 1). The structures were manufactured by Deep Reactive Ion Etching (DRIE) with the Bosch process: isotropic dry etching with sulfur hexafluoride, SF_6 at 2 °C cathode temperature, and sidewall passivation by polymer deposition with octafluorocyclobutane and oxygen, C_4F_8/O_2, in the tool Tegal 200 (SPTS) [4]. The deposition and etch time in each cycle were 1.0 and 1.8 s, respectively. The duration of total etch was 16 min. The different structure depths were achieved on the same wafer depending on the structure width based on the well-known aspect ratio depending etching (ARDE) effect.

The normal incidence reflectometry in the spectral range of 250–800 nm implemented in the wafer metrology tool KLA-Tencor Spectra Fx 200 was used for TSV characterizations. The optical objective with low numerical aperture (NA < 0.01, angle of incidence $\alpha \sim 88.23°$) and an illumination spot size of about 40 μm was utilized. The wavelengths resolution was approximately 1.25 nm at $\lambda = 775$ nm.

TSV depth was extracted from the interference effect between waves reflected from TSV's top and bottom surfaces [13]. The diffraction effect of light from sidewalls was analyzed in order to determine the scallop size. The rigorous coupled wave analysis (RCWA) based on light scattering with the commercial simulation software [14] is applied for TSV top and bottom CD and scallop amplitude evaluation. SEM measurements were used in order to prove our results.

Table 1
Geometrical parameters of single TSV structures from arrays obtained from spectral reflection (R) in comparison with SEM results.

Sample	1		2		3		4	
	R	SEM	R	SEM	R	SEM	R	SEM
Top CDx, μm	3.0	3.0	3.7	3.7	4	4.1	6.35	6.5
Top CDy, μm	3.1	3.1	3.6	3.6	5.1	5.1	7.15	7.1
Bottom CDx, μm	1.5	1.7	1.5	1.9	2.7	2.8	4.8	5
Bottom CDy, μm	1.5	n/a	1.5	n/a	3.8	n/a	5.6	n/a
CD super-ellipse power p	4		5		6		7	
Pitch x, μm	7.4		7.4		8		10.7	
Pitch y, μm	7		7.5		9.2		11.2	
Depth, μm	50.2	50.3	55.7	53.2	58.5	59	67.2	67.8
Top scallop period, nm	343	340	350	350	360	360	375	380
Top scallop amplitude, nm	85	85	98	90	102	95	103	98

3. Results and discussion

Fig. 1 shows SEM views of the investigated TSV array structures. Two types of surface texture can be observed on the TSV side walls formed by DRIE. The first type is the scalloping effect which is caused by the alternating isotropic etch and passivation steps in the Bosch process. The second type is a random sidewall roughness due to the ion behavior during etching. The sidewall scalloping (period as well as amplitude) gradually decreases with TSV depth, as shown in Figs. 1 and 2. Wall scalloping occurs primarily in the top region where scattered ions have wide trajectories, and less so in greater depths where ion trajectories are more restricted.

A decrease of the scallop amplitude with large TSV depth with a rapid slop in the TSV top part is observed. The behavior is similar for the different CDs (Fig. 2a). From 2/3 depths down to the bottom, small holes which are attributed to the isotropic etch attack in combination with small scallops have been observed. The presence of the deeper scallops corresponds to the large scallop period as well. But the reduction of the scallop period with the relative depth from the top of the TSV is sharper for smaller structural widths (Fig. 2b). Fig. 2 show the increase of scallop amplitude and period with TSV CD.

Considering the interaction of incident light with such structures, different reflection response can be expected from different CDs TSV structures.

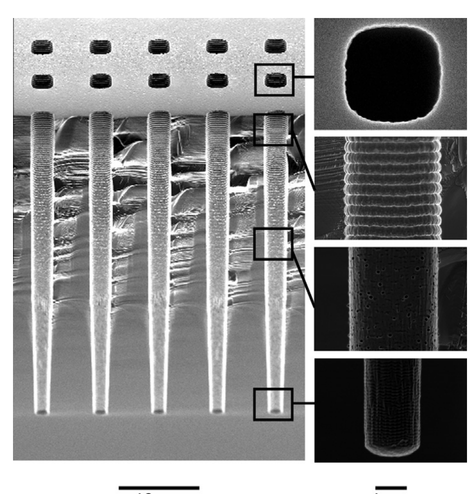

Fig. 1. SEM views of TSV array (top CD ≈ 3 μm, pitch ≈ 7 μm, depth ≈ 50 μm).