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Investigation of different methods for isolation in through silicon via for 3D integration

Stéphane Sage [a], Peggy John [b], Stephan Dobritz [b], Jochen Börnge [a], Julien Vitiello [a,*], Matthias Böttcher [b]

[a] Altatech, 611 Rue Aristide Bergès, Montbonnot 38330, France
[b] Fraunhofer Institute IZM-ASSID, Ringstr. 12, Moritzburg 01468, Germany

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ABSTRACT

3D integration is now a realistic, mainstream solution to tackle the issue of device scaling and achieve decreased RC delay times and reduced power consumption, by using through-silicon-vias (TSV). In this architecture, a via liner performs multiple functions as an insulator, a Cu diffusion barrier and an adhesion promoter. The dielectric layer is the key element in fulfilling the electrical requirements for TSV when a high aspect ratio of more than 5:1 is used. This paper presents a new methodology for creating a dielectric liner by using a dual plasma-enhanced/high-pressure chemical vapour deposition (PE/HPCVD) layer of SiO_2 to produce a better 3D integration solution than today's commonly used SiO_2 deposition process.

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1. Introduction

Three-dimensional integration is now a realistic, mainstream solution to tackle the issue of device scaling and achieve decreased RC delay times and reduced power consumption [1]. Using trough-silicon-vias (TSV) to fabricate 3D semiconductors enables high-density stacking with low-electrical-resistance connections between chips [2,3]. This technology would allow for packages that are smaller, consume less power, and perform significantly faster.

Whether using a via-first or via-last approach, the TSV integration scheme is based on three main steps: via creation, via liner deposition and via filling [4]. The via liner performs multiple functions as an insulator, a Cu diffusion barrier and an adhesion promoter. It consists primarily of a metallic seed barrier and a thicker SiO_2 dielectric liner (Fig. 1).

Depositing the via liner is a critical middle step in which any defects that may result from etching a deep via through silicon must be corrected or covered. The SiO_2 dielectric liner itself should have sufficient insulating capabilities, while the vias width must be maintained to enable the subsequent via-filling step using metallic barrier and copper (Cu) sputtering processes, followed by electroplating step. Moreover, the dielectric liner must smoothen the via wall surface in order to facilitate the next integration steps, such as metallic barrier deposition and Cu filling. The dielectric liner is the key element in fulfilling the electrical requirements for TSVs when a high aspect ratio (more than 5:1) is used.

In the case of via-last TSVs, the dielectric liner must fulfil these three criterions:

- Be deposited in a conformal way, despite the high aspect ratio.
- Ensure sufficient insulation properties to avoid leakage current with adjacent vias, thanks to an optimized thickness/insulating properties ratio.
- Be deposited at low temperature (lower than 350 °C) because of the via-last integration, in order not to damage the chips present on the wafers.

Each one of these criterions, considered separately, can be addressed today through standard oxide deposition techniques such as PECVD (plasma enhanced), HPCVD (high pressure), LPCVD (low pressure), APCVD (atmospheric pressure), etc. But to address the three criterions altogether, no satisfying solution exists. The LPCVD technique allows to obtain an excellent quality oxide layer (dielectric properties, uniformity) but with a low deposition rate and a very high deposition temperature for the considered application (>500 °C). The APCVD technique does not allow growing a good quality layer at temperatures lower than 400 °C and has a low deposition rate. The PECVD deposition shows a high deposition rate and enables to work at low temperature thanks to the plasma assistance, but does not allow to fill high aspect ratio vias in a conformal way. Lastly, the HPCVD exhibits a very good conformality, is compatible with low temperature, but the oxide layers have poorer dielectric properties. Because of this, for high aspect ratio vias, obtaining a layer that shows good dimensional and electrical characteristics from the top to the bottom of the vias is very challenging [5].

* Corresponding author.
E-mail address: julien.vitiello@altatech-sc.com (J. Vitiello).

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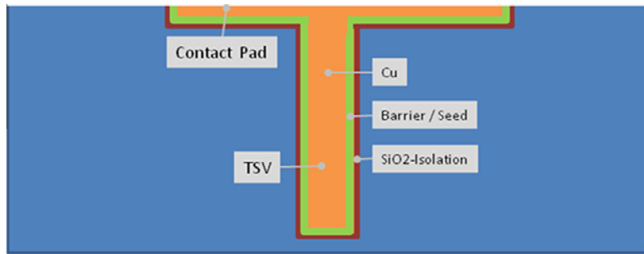

Fig. 1. TSV-structure of the IZM-ASSID test chip for 3D-integration.

This paper investigates standard PECVD and HPCVD processes and presents a new methodology for creating a dielectric liner: using a dual plasma-enhanced/high-pressure chemical vapour deposition (PE/HPCVD) layer of SiO_2. The target is to produce a better 3D integration solution than today's commonly used SiO_2 deposition process, by combining the dielectric performances of PECVD oxide and conformality of HPCVD oxide.

2. Experiments

This study has been performed using a 300 mm dual PE/HPCVD AltaCVD® reactor manufactured by Altatech®. It has the capability to perform pure CVD deposition (HPCVD, with O_3 reactive gas) as well as plasma-enhanced CVD deposition (PECVD, with O_2 reactive gas). This flexibility allows to perform depositions consisting of a combination of PECVD and HPCVD processes in the same reactor, without air break.

The TSVs, manufactured on 300 mm wafers, are 10 µm wide and 100 µm deep (10:1 aspect ratio). They are etched using a deep silicon etch process, then the dielectric liner is deposited using TEOS chemistry, followed by metallic barrier deposition (TiN or Ta/TaN), seed copper sputtering and copper electroplating. A TEOS precursor was chosen for SiO_2 deposition because, as already shown with different reactors [6,7], it presents many advantages over silane. Fig. 2 illustrates the lower overhang, superior step coverage and smoother surface obtained using TEOS chemistry.

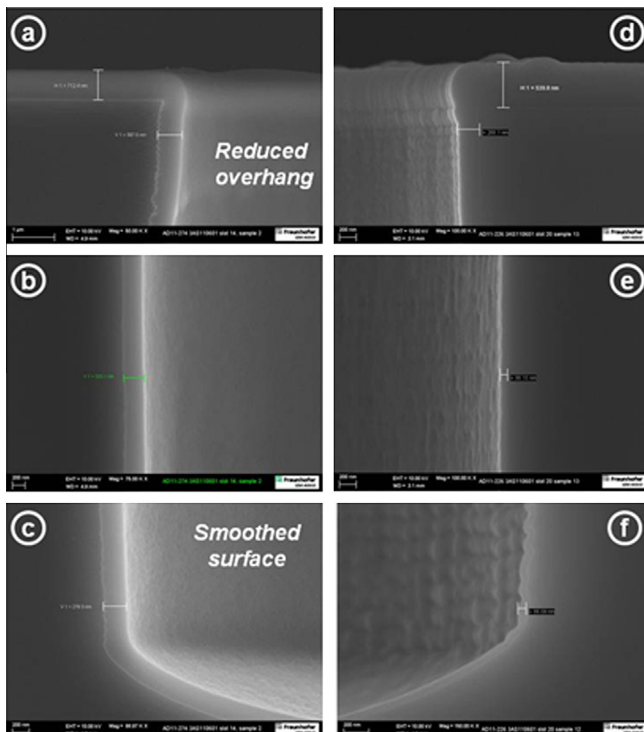

Fig. 2. SEM cross-section of TSVs after dielectric liner deposition with TEOS (a–c) and silane (d–f) chemistry.

Table 1
Main characteristics of the standard PECVD and HPCVD processes used in this study.

	HPCVD	PECVD
Temperature (°C)	350	350
Pressure (torr)	>100	2–10
Plasma	No	Yes
Gases and precursors	He, O3, Teos	He, O2, Teos
Deposition rate (nm/min)	200	510
Uniformity (% 1σ)	1.6	1.75

Table 2
Wafers processed for the *C–V* tests.

Wafer #	Process	Temperature (°C)	Thickness (nm)
1	Thermal oxide	1000	100
2	PECVD	350	100
3	HPCVD	350	200
4	HPCVD + PECVD	350	100 + 100
5	PECVD + HPCVD	350	100 + 100
6	PECVD + HPCVD	350	50 + 150

A description of the two processes investigated in this study is shown in Table 1. Thickness and its uniformity across the 300 mm wafers were measured using a reflectometer. Uniformity values are given in 1σ percentage and correspond to 49 points measurements with a 5 mm edge exclusion.

The step coverage across the TSVs height was measured using a SEM microscope. Table 2 shows the processes that were used to perform SiO_2 depositions on the test wafers and then characterized.

For electrical characterizations, IZM-ASSID test chip (ATEC) has been used. It covers specific test fields for process characterizations in all lithographic processes, TSV etch, barrier/seed deposition, interlayer dielectric and metal deposition on both wafer sides. The concept allows easy and flexible exchange of layers for different requirements. The basic reticle size is 30 × 30 mm^2 and it is divided into nine different substructures which can be separated and assembled in different variations.

The electrical characterizations of the dielectric layers were performed on contact pad structures (1 mm × 1 mm × 2.4 µm) made with the same succession of processes as the TSVs. *C–V* measurements were performed with the bulk of the silicon as the ground and the capacitance was measured on each of the 64 pads at a frequency of 1 MHz.

3. Results and discussion

3.1. Conformality

As expected, with such high aspect ratio TSVs and low deposition temperature (350°), PECVD showed poor conformality. On the contrary, HPCVD at 350 °C enabled to deposit nearly half of the top thickness at the bottom of the vias. The next step was to perform depositions combining the two processes. A dielectric liner was deposited through a PECVD deposition followed by a HPCVD deposition at 350 °C in a single recipe. The deposition times were adjusted to have about half of the top thickness deposited by each process. The succession of HPCVD and PECVD was also tested.

The results are summarized in Table 3. The dual PE/HPCVD process is much better than the pure PECVD one, with a conformality nearly tripled at the bottom of the via, and one third of the top

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