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Atomic layer deposition for high aspect ratio through silicon vias

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ABSTRACT

The paper presents atomic layer deposition (ALD) processes and process integration for the deposition of insulating liners, copper diffusion barriers, and seed layers for direct copper plating in high aspect ratio (>20:1) through silicon vias. A TaN-based copper diffusion barrier was deployed on an aluminum oxide insulating liner. The latter has the potential to act also as a dielectric barrier against copper diffusion according to BTS and TVS measurements. Furthermore, ruthenium ALD films applied as seed layers for direct copper plating were deposited with an intermediate annealing step to improve film adhesion and ensure the deposition of thick films without any delamination. The step coverage of the presented ALD processes was confirmed by SEM measurements on cross-sections of coated TSV structures. Finally a subsequent electrochemical deposition (ECD) of copper was conducted revealing the satisfying functionality of the Ru seed layer.

1. Introduction

The fabrication of high aspect ratio through silicon vias (TSVs) will be essential for future 3D interconnect technology, advanced chip-to-chip communication and a more efficient packaging. While low aspect ratio TSVs (<10:1) are already in the market, the research and development efforts on high aspect ratio TSVs are still on a high level to allow processing of thicker silicon wafers or to realize vias with lower diameters for lower surface consumption and reduced TSV volumes [1]. Since high aspect ratio approaches using tungsten chemical vapor deposition (CVD) are limited on annular or trench structures to achieve a sufficient conformality [2], atomic layer deposition (ALD) offers a diversity of materials and processes assuring suitable conformality within a limited thermal budget even for high aspect ratios [3,4]. In this paper, we show the fabrication of high aspect ratio TSV structures based on ALD film stacks working as insulating liner, copper diffusion barrier and seed layer for direct plating of copper. The TSV fabrication is presented as a proof of concept with the main focus on the employed ALD processes, films, and related challenges especially regarding the ruthenium seed layers. Finally, the TSV structures were subsequently coated with copper using an ECD process and analyzed to prove the functionality of the Ru seed layer.

2. Materials and methods

The ALD processes were carried out in an ALD cluster tool with two process chambers for 300 mm wafer, one of them with a bank of lamps for rapid thermal processing (RTP), various in situ analytics for advanced process control and a connected ultra high vacuum surface analysis system for film characterization without vacuum break [5,6]. The employed ALD processes described below were conducted at substrate temperatures between 200 °C and 250 °C without any vacuum break. The TSV test structures were prepared by Bosch-based reactive ion etching (RIE) processes [7,8] and the electrochemical deposition of copper was carried out as a galvanostatic deposition with Intervia Viafill® electrolyte containing a mixture of three proprietary organic additives (accelerator, suppressor, and leveler).

2.1. Insulating liner

Aluminum oxide (Al_2O_3) ALD films were deposited as insulating liners in a cross-flow ALD chamber using trimethylaluminium (TMA) from a cooled vaporizer (16 °C) as aluminum source and water as oxidizing agent separated by Ar purging steps [9–11]. The Al_2O_3 processes with 400 sccm Ar carrier and purge gas flows and a working pressure of 80 Pa result in a film growth of ~0.1 nm per cycle (GPC) with a cycle time of 6 s which enables sufficient throughput even for high film thicknesses which are needed for proper isolation and reduced parasitic capacitances to minimize RC delays. The electrical characterization of as-deposited Al_2O_3

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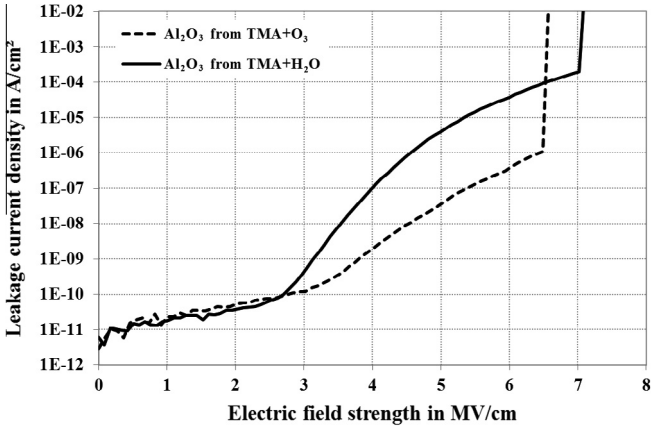

Fig. 1. Current–voltage-measurements on planar metal–insulator-metal (MIM) capacitors with Al_2O_3 dielectrics (from TMA + H_2O and TMA + O_3) and titanium based electrodes proofing low leakage currents (<0.1 nA/cm^2 at 2 MV/cm) and high breakdown field strengths (>6 MV/cm).

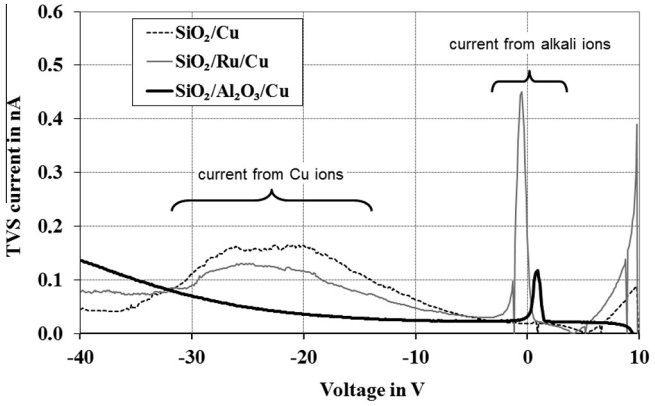

Fig. 2. Triangular voltage sweep (TVS) measurement of metal–insulator-silicon (MIS) structures with 15 nm Al_2O_3 applied as dielectric barrier against copper diffusion in comparison to structures without or with a ruthenium-based copper diffusion barrier.

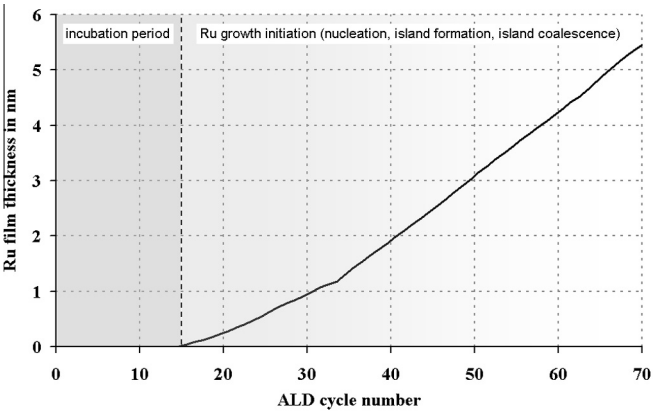

Fig. 3. Incubation period and Ru film growth initiation on a tantalum nitride-based surface measured during deposition with in situ spectroscopic ellipsometry.

ALD films using planar metal–insulator-metal (MIM) capacitors with titanium based electrodes (see Fig. 1) proofed low leakage currents of less than 0.1 nA/cm^2 at 2 MV/cm and high breakdown field strengths of about 7 MV/cm which are consistent with

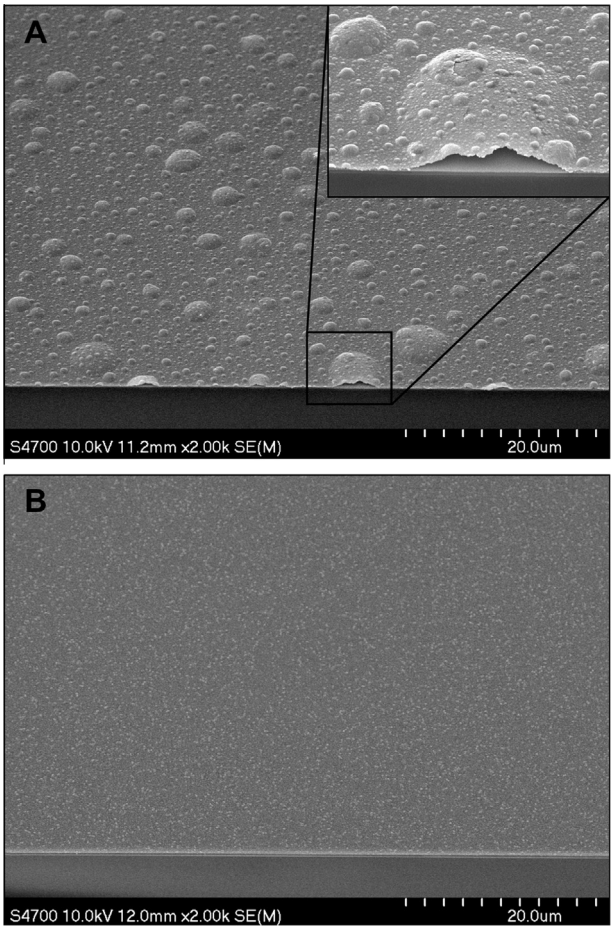

Fig. 4. Comparison between a delaminating 25 nm Ru film (A) and a 25 nm Ru film on TaN with an intermediate annealing step (10 min at 600 °C) carried out after deposition of the first 5 nm (B).

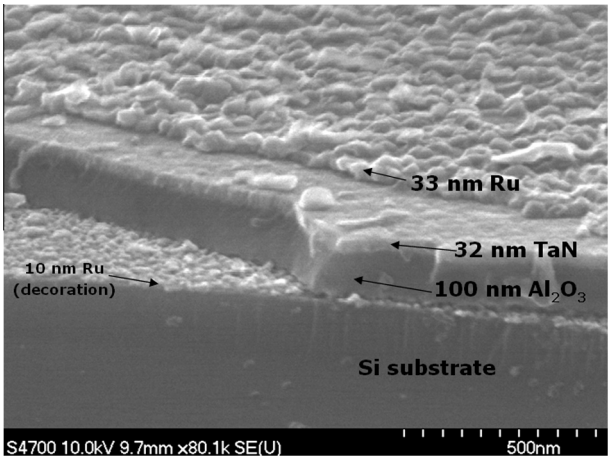

Fig. 5. SEM cross-section detailing the applied ALD film stack on the wafer surface.

reported values for amorphous Al_2O_3 films [12] and similar to own values obtained with films from an ozone based Al_2O_3 ALD process. Furthermore, metal insulator silicon (MIS) test structures with 15 nm Al_2O_3 films (annealed for 1 h at 300 °C in H_2/N_2) have been successfully tested on their copper diffusion barrier properties by means of bias temperature stress (BTS) - 30 min at 250 °C with an applied electric field of 2 MV/cm - followed by triangular