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Reliability of chip on glass module fabricated with direct printing method

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ABSTRACT

To investigate the effect of the sintering temperature on the electrical properties of a chip on glass (COG) module, a screen-printed conductive circuit was sintered at various temperatures, viz. 150, 200, 250 and 300 °C for 30 min. An anisotropic conductive film (ACF) is a suitable bonding material for the interconnection between a device and printed circuit, because of the conductive particles within it. We expected that the conductive particles in the ACF would provide a good electrical connection and reliability in our study. The electrical properties of the printed Ag circuits improved with increasing sintering temperature. The conductive particles in the ACF were well deformed in between the Au bumps and printed Ag pads after the bonding process. The resistances of the interconnections drastically decreased with increasing sintering temperature. Also, the temperature–humidity reliability of the ACF was investigated by measuring the resistance after the temperature–humidity test (THT) at 85 °C and 85% relative humidity. After the THT, the resistance shows a tendency to decrease when sintered below 200 °C, whereas it increases when sintered over 250 °C. The increase in the resistance due to the effect of surface oxidation is negligible.

1. Introduction

Various printing technologies, e.g., the ink-jet, roll based and screen printing methods, have been proposed as alternatives for the patterning of conductive, semi-conductive or insulating materials on account of their low-cost, large-area patternability and pattern flexibility [1,2]. Printed electronics has its origins in the conductive patterns printed as part of conventional electronics, forming flexible keypads [3], antennas [4,5], radio frequency identification tags [5–7] and so on. Then came fully printed testers on batteries, electronic skin patches and other devices made entirely by printing, including batteries and displays. A clear next step has to be the modernization of the fabrication process of semiconductor chips, e.g., various capacitor chips, central processing units or driver integrated circuits (ICs) for displays, by making use of printing technologies.

Herein, we attempted to utilize a printing technique, i.e., the screen printing method, to form a conductive circuit on a dummy chip to test the reliability of a 'chip on glass' bonded by an anisotropic conductive film (ACF). The materials used for the printing chosen herein was a highly viscous paste containing Ag nanoparticles, which was screen printed onto a Si substrate to form an electrical circuit for testing. Si chips with Ag patterns were attached to a glass panel with an ACF. ACF is a well-known bonding material that consists of an insulating adhesive polymer matrix with a specific loading of conductive particles (5–10 wt.%). It provides unidirectional conductivity in the vertical or *z*-direction (perpendicular to the plane of the substrate) [8]. The concentration of particles is controlled so that sufficient particles are present to ensure reliable electrical conductivity between the assembled parts in the *z*-direction, while insufficient particles are present to achieve percolation conduction in the *x*–*y* plane [9]. For these reasons, we considered that an ACF is a suitable bonding material for the interconnection between the device and printed Ag circuit, because of the conductive particles within it. We expected that the conductive particles in the ACF would provide a good electrical connection and reliability in our case of study.

In this study, we investigated the feasibility of using printing methods to fabricate directly printed integrated circuits and their reliability in a type of flip chip assembly employing an ACF for bonding. It should be noted that photo-lithography followed by a harmful metal etching process is the generally accepted way to make a specific pattern in the industry. At this point, the reliability of the adhesion layer has been considered to be the major issue, whereas the major issues to be resolved when employing the printing method for circuit fabrication are unknown. Therefore, we firstly fabricated the chip on a glass module by screen printing Ag nanopaste and by applying the ACF, and then verified its reliability using a high temperature and humidity test (THT) chamber. After storing them in the chamber, we analyzed various aspects of the samples by scanning electron microscopy and X-ray diffraction,

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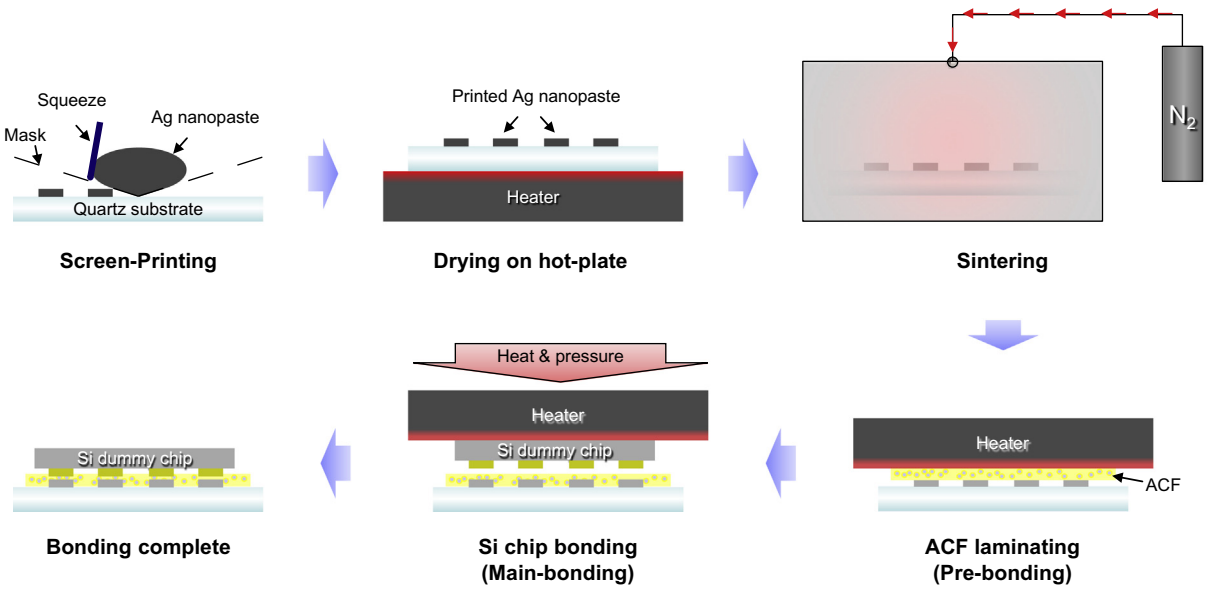

Fig. 1. Schematic illustration of screen-printing and bonding process.

focusing especially on the printed circuits and the adhesive interconnection.

2. Experimental procedures

We used 4 inch diameter and 500 μm thick silicon wafers for the fabrication of the Si dummy chip. The SiO_2 passivated Si wafer was sputtered with 0.2 μm thick Ti as the adhesion layer and 0.8 μm thick Cu as the seed layer for plating, respectively. After the first photo-lithography (PL) process, Au was electroplated on the sputtered Cu. A commercial plating solution (TEMPERESIST EX-3000, JAPANPURE CHEMICAL Co., Ltd., JAPAN) was used for the deposition of the Au bump. The temperature of the solution was kept at 50 °C by means of a heater situated underneath the electroplating tank with mechanical stirring. An approximately 10 μm-thick layer of Au was electroplated in a bath at a current density of 0.5 ASD (A/dm^2) for 30 min. The second PL processes were employed for patterning the Cu tracks on the Si wafer. The number of Si chips per wafer was 100 EA, the total number of Au bumps per chip was 160 EA, and the dimension of chip is 4×4 mm. The Au bumps on the patterned wafers were arranged at a pitch of 200 μm with a square-shaped bump opening area of $80 \times 80\ \mu m^2$. To measure the connection resistance, the Kelvin structure was designed. With the Kelvin method, we could detect the electrical resistance only within the interconnection layer.

We employed an Ag nanopaste consisting of $20 \sim 50$ nm sized Ag nanoparticles dispersed in an α-Terpineol matrix. The solid loading level of the Ag conductive paste was about 55 wt.%. The thickness of the stencil mask was 49 μm and a 400 mesh stencil mask was used. Here, the mesh count was 400, which means the number of holes per square inch. The fabrication process of the COG module with the direct printing method is shown in Fig. 1. Firstly, we diced a 6 inch quartz wafer into a rectangle, because the printed circuits were frequently delaminated during the dicing process. The squeezing pressure and speed were 195 MPa and 300 mm/s, respectively. The printed Ag circuits were immediately fully dried on a hotplate at 70 °C and then sintered in a rapid thermal annealing furnace (RTA-BRT100, BLS Co., Korea). To investigate the effect of the sintering temperature, various sintering temperatures were used, viz. 150, 200, 250, and 300 °C, in an N_2 atmosphere for 30 min. To package the Si dummy chip on the quartz substrate, we employed an ACF which is a film type of adhesive.

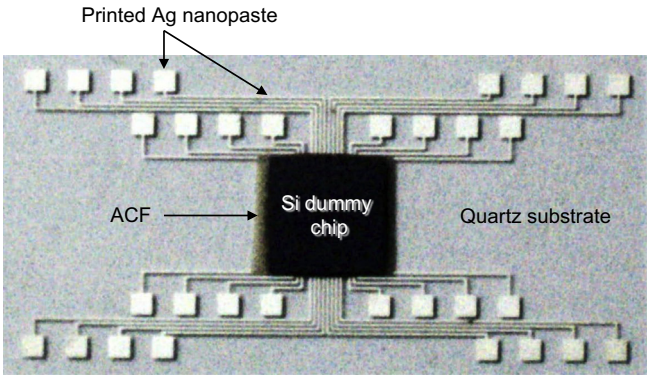

Fig. 2. Top view of bonding completed COG module.

The ACF (Sony Chemical & Information device Corp., Japan) used in this study was of the thermosetting epoxy type with a thickness of 30 μm consisting of 10 μm-diameter conductive particles. The conductive particles were polymeric cores coated with Ni and Au. Before the main flip chip bonding of the Si dummy chip on the substrate, the pre-bonding of the ACF on the substrate was conducted with a force of 10 N and a temperature of 75 °C for 3 s, as shown in Fig. 1. A Laurier Flip Chip Bonder (M9-A, Laurier, USA) was used to join the flip chip to the substrate. The main bonding process was conducted at 30 N and 180 °C for 10 s. The ramping temperature rate was 6 °C/s and the cooling rate was 1.8 °C/s. Fig. 2 shows the COG module after the completion of the bonding process. To investigate the reliability of the COG module under high temperature and humidity environmental conditions, five samples for each condition were put in the THT (85 °C/85% relative humidity) chamber (PSL-2KTH, ESPEC, JAPAN) for 50, 100, 300 and 500 h.

The surface and fractured internal microstructures of the printed Ag circuits sintered at various temperatures were observed by field emission scanning electron microscopy (FE-SEM). A cross-section study was conducted through the outer array of Au bumps. The microstructural observations were made using FE-SEM. The resistance of the COG module was measured on five samples for each condition using a four-point probe method and the average