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Investigation of solder crack behavior and fatigue life of the power module on different thermal cycling period

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ABSTRACT

With the continuous expansion of high-power electronic product applications, the high resistance of power modules to cyclic current loading has become a major concern. The heat generated by a chip during operation causes the power module's temperature to vary rapidly. Many accelerated tests are required to understand the effect of temperature loading on the power module and its reliability. One is the power cycling test. The international regulation for the test suggests the test condition, that is, the difference between the maximum and minimum junction temperatures during one power cycle, should be identified. Nevertheless, the cycling period is within the range of 1-15 min. To understand the relationship between cycling period and power module reliability, the modules were subjected to thermal cycling between -40 and 125 °C with 66 and 30 min cycling periods. The solder crack was measured after a certain number of thermal cycles. In addition, to determine the initial crack life, this research extrapolated the average crack length in terms of the number of thermal cycles. The results show that the solder height variation significantly affected the crack growth. Therefore, the study focused on solders with heights between 150 and 300 μm and exceeding 300 μm to minimize the effect. The results show that the life of the initial crack and crack growth rate for the solders with heights between 150 and 300 µm were 37 cycles and 0.0114 mm/cycle respectively. Almost no crack initiation was found among solders with heights exceeding 300 µm. Besides, the longer thermal cycling period caused a significantly shorter initial crack life and higher crack growth rate than the shorter cycling period. The findings could be attributed to the phenomenon that increasing thermal cycling period brought more creep strain and inelastic strain energy density.

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1. Introduction

Power modules have been widely applied in various electrical products such as power supplies, uninterruptible power systems, DC/DC converters, and hybrid vehicles. With the increasing demand for high power, highly reliable, advanced power modules have become an inevitable issue. Fig. 1(a) shows the schematic of a power module. The pad is deposited on the active region of the insulated gate bipolar transistor (IGBT) chip, which is mounted on the direct copper-bonded (DCB) substrate with the 96.5Sn-3.5Ag solder. Then, the DCB substrate is attached to the copper plate through the 96.5Sn-3.5Ag solder. After the substrate assem-

* Corresponding author at: Department of Power Mechanical Engineering, National Tsing Hua University, HsinChu 300, Taiwan, ROC. Tel.: +886 3 5742925; fax: +886 3 5745377. bly, the wire is bonded to the pad surface using the ultrasonic wedge bonding technology. Finally, the module is assembled. The heat generated by a chip during operation causes the power module's temperature to vary. Although packaging technology with DCB substrates is known as an effective potential solution for its remarkable heat dissipation, major problems on thermally induced stress continue to exist. Fig. 1(b) shows that the solder is a weak point in the power module. The accumulated inelastic strain from the coefficient of thermal expansion (CTE) mismatch between the chip and DCB substrate can cause solder fatigue. The stress concentration in the solder due to the CTE mismatch between the DCB substrate and copper plate can also cause solder failure [1–3].

Many studies have focused on evaluating the reliability of power modules during operation [4–6]. One typical method for such assessment is the power cycling test, related regulations have been published by the International Electrotechnical Commission



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Fig. 1. (a) Schematic of the power module; (b) solder fatigue.

[7]. This test has been widely adopted for investigating the effects of cyclic current loading on the power module and its reliability assessment. Several test conditions for regulating the difference between the maximum and minimum junction temperatures during one power cycle can be used. However, the cycling period is within the range of 1–15 min, as shown in Fig. 2. A long cycling period may induce a large inelastic strain and accelerate solder crack initiation and growth. To understand the relationship between the cycling period and power module reliability, the modules (Fig. 3) were subjected to thermal cycling between -40 and 125 °C with 66 and 30 min cycling periods. This paper presents the results of the crack observation during the thermal cycling test. For several thermal cycles, the power modules were removed from



Fig. 2. Temperature profile in one test condition.

the thermal chamber and the crack lengths were measured using a scanning acoustic microscope (C-SAM).

2. Solder failure mechanism

As shown in Fig. 1(b), the power module consists of two leadfree solder layers treated as bond layers. This study focuses on the failure mechanism of the solder between the DCB substrate and copper plate. The temperature distribution and CTE mismatches between the DCB substrate and copper plate induce inelastic strains at the solder, which may further result in fatigue failure. Several studies [8,9] have shown that cracks initiate at the solder boundaries and grow throughout the bond layers. The solder failure mechanism can be represented by the Darveaux constitutive model shown in Eqs. (1) and (2) [10]:

$$N_0 = C_1 \Delta W^{C2} \tag{1}$$

$$\frac{da}{dN} = C_3 \Delta W^{C4} \tag{2}$$

where N_0 is the number of thermal or power cycles before crack initiation, $\frac{da}{dN}$ is the crack growth per cycle, ΔW is the inelastic strain energy density per cycle in the solder, and C_1 , C_2 , C_3 , and C_4 are undermined constants identified by the experiment correlation. The number of cycles before crack initiation and crack growth per cycle can be calculated using Eqs. (1) and (2), respectively. The number of cycles to failure can be described by the following equation:

$$N_f = N_0 + \frac{L}{da/dN} = N_0 + N_{II}$$
(3)

where *L* is the critical crack length when the failure event is determined and N_{II} is the number of cycles associated with crack growth. Conventionally, solder height affects crack growth [11,12]. The non-uniformity of the solder layer may influence the crack growth rate and power module reliability. Therefore, a method for minimizing the non-uniformity effect is needed to investigate the crack initiation and growth.

3. Solder height observation

In view of the previous section, the variations in solder height between the copper plate and DCB substrate must therefore be determined. As described in Fig. 4, one power module has three DCB substrates. The power modules were cross-sectioned, and 12 locations were examined to observe the solder height. The instrument was focused on the near corner of the DCB substrate for the solder height measurement. Fig. 5 shows the substantial differences in solder height. Moreover, based on 204 solders, the variation covers a very wide range (low stand-off height <100 µm, high stand-off height >300 μm). This wide variation can be caused by factors such as non-uniform solder paste, temperature, and supporting weight, etc. Generally, after the surfaces are mounted, the solder height should be above 150 µm. However, an efficient surface mounting technique for forming uniform solders has not been established until now. The following section describes the effect of solder height on crack growth.

4. Crack length measurement

The power modules were subjected to thermal cycling between -40 and 125 °C with 66 and 30 min cycling periods. After several thermal cycles, the solder crack length was measured using C-SAM. Fig. 6 illustrates the crack length after a certain number of thermal cycles. As shown, the crack length progressively

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