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Modeling and simulation of the interplay between contact metallization and stress liner technologies for strained silicon

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ABSTRACT

The interplay between the performance of nitride stress liner technologies and the contact metallization is studied based on computer simulations. Three dimensional models of transistor devices including the contacts have been created for the 32 nm and 45 nm technology nodes. The loss of stressor performance by opening the contact holes is studied systematically as function of the contact width. The use of strained contact metals to recover the performance loss due to metallization is demonstrated for nFET devices based on the simulation results.

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1. Introduction

Strained silicon has become one of the key enabling technologies for improving the performance of transistors in state-of-the-art ultra-large-scale integrated devices. In order to strain the semiconductor material in the transistor channel, usually several stressors are integrated such as strained plasma enhanced nitride (PEN) liners, strained SiGe pockets or various stress memorization techniques [1–8]. For contact metallization, however, the PEN-liner must be opened to bring in the contact hole and thus, the stress will be released and the transistor performance gain due to the stressor is partially lost. In the present paper we will focus on the complex interplay of strained PEN liners and the contact metallization system.

Measuring the local stress or stress distributions in the nanoscaled transistor channels is a challenging task. First direct measurements of the strain distribution in the transistor channel have been demonstrated but are still far from routine use [9,10]. Thus, simulation is up to now the only method to analyze the function of the different stressor technologies in a systematic way [11,12].

Although a few simulations on various aspects of the stressor performance exists in literature [9,10], the interplay between stress liner and contact metallization has not been analyzed so far. In the present paper we will show that a common modeling and simulation analysis of both, the PEN-liner and the metal contact provides new insights into the mechanisms of the stressor performance and how it is degraded by the contact formation.

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2. Model details

A three dimensional model of state-of-the-art transistors has been developed using the Synopsys® Sentaurus TCAD package. In the first step, a geometric transistor model is created using Synopsys® Sentaurus Structure Editor. The model is parameterized in such a way, that all relevant dimensions can be chosen freely. The dimensions of the transistor models are taken from device cross sections which were measured by electron microscopy on samples from fully processed wafers. This approach allows us to model the transistor devices as realistic as possible for all relevant technology nodes, currently including the nodes 28, 32 and 45 nm. Table 1 summarizes some critical dimensions which were used for the simulation models for the 32 and 45 nm node. The given intervals reflect the typical variability due to process- and design related fluctuations.

In order to compute the stress distribution in the materials, a process flow consisting of strained PEN-liner deposition, TEOS deposition, contact etch and strained tungsten fill is modeled using Synopsys® Sentaurus Process in a second step. During the process flow, in all process steps, the equations of thermo mechanics are solved on a grid resulting in a model of the stress distribution within the transistor. The strained PEN-liner is modeled such, that the strained layer is deposited within one step and the whole structure is allowed to relax mechanically afterwards. This procedure has demonstrated to give realistic results for tensile strained liners used for the nFETs, where mechanical stress is created basically due to the mismatch of the thermal expansion coefficients and by the liner material shrinkage due to succeeding curing processes. In contrast, the compressive liners used for the pFETs, are best modeled by subdividing the liner deposition in a series of 20

Table 1
Overview of critical structure dimensions. All values are given in nm.

	32 nm		45 nm	
	nFET	pFET	nFET	pFET
Gate length	30–37	30–37	40–47	40–47
Gate height	55–65	55–65	63–75	63–75
Spacer width	6–8	6–8	30–37	30–37
PEN thickness	23–27	40–48	32–37	36–44
Recess etch depth	0–7	0–7	0–10	0–10
Contact width	35–45	35–45	55–65	55–65

deposition/relaxation steps [13]. This is due to the fact, that for compressive nitride liners the stress is developing while the material grows. Throughout the simulations shown in this paper, the stress in the PEN was set to a value of 2 GPa for the nFETs and to −3 GPa for the pFETS.

For simplicity we regard only source and drain contacts and the transistor structure itself is extruded along the z-axis. Contacts are modeled to have an oval cross section with a finite depth. We define the contact width w_{con} such that the cross section becomes circular when the width approaches the length of the contact. Contact lengths are 40 nm in the 28/32 nm technology and 60 nm in the 45 nm technology. Strained tungsten contacts are modeled in a similar way as the stress liner. After filling the contact holes, the stress of the contact material is set to a fixed value and the structure is allowed to relax again. The default value of the tensile stress in tungsten is set to 1.6 GPa which is a typical value found when the metal is deposited on blanket wafers under conditions identical to those for the contact formation.

Due to the lack of concepts to model circular structures in Sentaurus Process when etching the contact holes virtually within the simulated process flow, the contacts where modeled with a polygonal cross section. The number of corners was varied systematically and convergence of the simulation results was observed when the number of corners was increased from 8 to 16.

The overall model consists of three neighboring transistors along the x-axis (channel direction) with distances according to the pitch of the respective technology node. Only the half structures are actually computed due to symmetry reasons. Reflective boundary conditions are used along the x-direction while in y-direction the interfaces of the model are free. Along the z-axis, which is the direction perpendicular to the channel within the wafer plane, the model is cut at a fixed position. Together with reflective boundary conditions this cut-off can be used to model periodically repeated structures in z-direction. Again only half structures are regarded due to symmetry. We refer the half model width in-z-direction as z-pitch and its default value is set to 700 nm. Note, that the distance of two contacts in z-direction is twice the z-pitch. Fig. 1 shows the 3D-model of a 32 nm nFET structure including contacts. The simulation of three dimensional structures by finite element methods is very time and memory consuming compared to the two dimensional case. Thus, the simulation grid was optimized in order to keep the number of nodes as small as possible while still achieving a high accuracy of the results.

Based on this model, the stress distribution in the whole device can be computed for a given set of geometrical parameters and given values of the stress in the PEN-liner and the contact. In order to evaluate the transistor performance, we take the width averaged stress σ in the middle of the channel, directly under the gate oxide, as a figure of merit. For width averaging, the stress from a 150 nm wide interval around the center of the structure is integrated numerically along the z-axis and is divided by the interval width. The width of the averaging interval is chosen such, that it is close to the typical width of the transistor channel and we thus model

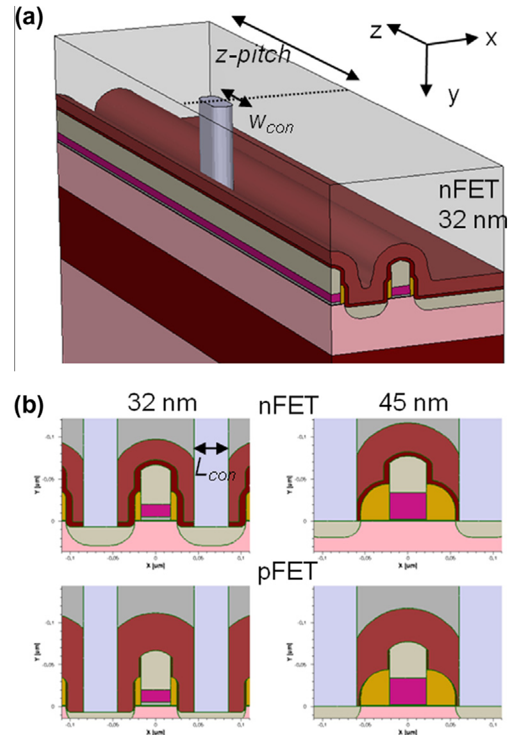

Fig. 1. 3D-model for transistor devices. (a) 3D-view of the nFET 32 nm model. Contact width and z-pitch are indicated by arrows. (b) Cross-sections of the structures of nFET and pFET devices in the 32 nm and 45 nm technology node.

a situation close to that found in a real transistor. The strain distributions along the channel appear comparably flat and thus no averaging has to be taken into account along the x-direction. From the z-averaged stress components σ_{xx}, σ_{yy} and σ_{zz} we compute the relative electron mobility change μ_{rel} as the ratio of the mobility in the strained and unstrained silicon. A simple piezo resistivity model for the electrons and holes [14].

$$\mu_{rel,e} = 1 + 0.314 \cdot \sigma_{xx} - 0.534 \cdot \sigma_{yy} + 0.178 \cdot \sigma_{zz}$$
$$\mu_{rel,h} = 1 - 0.718 \cdot \sigma_{xx} + 0.066 \cdot \sigma_{yy} + 0.718 \cdot \sigma_{zz}$$

was used as a measure of the transistor performance. The increase of the transistor current due to the strained silicon will be approximately proportional to the relative mobility change. In a series of device simulations on a similar 2D transistor structure using the more complicated state-of-the-art device models for strained transistors available in Synopsys Sentaurus Device, we could verify, that the simple piezo resistivity approach in combination with considering only the peak stress in the middle of the device gives reliable estimates of the transistor performance change.

The simulation model is based on mechanical data of the nitride films, the etch stop oxide and spacer nitride which are obtained using state of the art mechanical testing on blanket wafers (see Table 2). All other elastic data are standard values taken from the materials library provided by Synopsys along with the TCAD-Suite. With the exception of the modulus of silicon all involved material properties are isotropic. The mechanical properties of the involved

Table 2
Bulk modulus K and shear modulus G of the involved films.

	K	G
Spacer Nitride	160	73.8
Etch stop oxide	36.7	27.5
PEN	142	65.4

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