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Atom probe tomography of SRAM transistors: Specimen preparation methods and analysis

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ABSTRACT

Different FIB-based sample preparation methods for atom probe analysis of transistors have been proposed and discussed. A special procedure, involving device deprocessing, has been used to analyze by APT a sub-30 nm transistor extracted from a SRAM device. The analysis provides three dimensional compositions of Ni-silicide contact, metal gate and high-k oxide of the transistor gate.

1. Introduction

With the continuous scaling down of devices, the characteristic size of metal–oxide–semiconductor field effect transistors (MOSFETs) is now below 30 nm. The reliability and performance of the MOSFET is more and more a serious problem at this scale [1]. There are many factors that influence the characteristics of transistors and make the understanding of the origin of the reliability and performance quite difficult.

For example, local atom distributions have an ever more important impact on the electrical characteristics of individual devices: the distribution of dopants at the nanoscale affects locally the electrical characteristics and contamination with a few or even single impurities can also render unstable the transistor characteristics. In addition, as the device size decreases, the strain and stress fields play an increasing role in microelectronic devices for example by changing the carrier mobility. They can also affect the contact fabrication by changing the silicide formation mechanism and the alloy elements redistribution. Finally, the increasingly complex gate stack structure, with metal gate and high-k dielectrics, introduces many new interfaces and potential sources of channel mobility degradation [2].

With the actual dimensions of the transistors in devices, there is an increasing need for structural and chemical characterization at the subnanometer scale that cannot be fulfilled by standard techniques such as transmission electron microscopy (TEM) and secondary ion mass spectrometry (SIMS). Since the properties of devices depend on the three dimensional (3D) chemical composition, there is also a need for a 3D characterization of the devices at the nanometer scale. In addition, with the increasing number of interfaces in the transistor, dopant and impurities element segregation and/or precipitation interfaces [3] and also at defects should play an increasing role in the device performance [4]. These phenomena can be quantified by atom probe tomography measurement [5–7].

Indeed, atom probe tomography (APT) is a powerful tool to characterize internal interfaces and layer chemistry [8] with subnanometer scale resolution in three dimensions. For APT, the sample is prepared in a tip shape in order to create the very high electric field needed to field-evaporate atoms. The fabrication of such sample is generally a critical step for the APT analysis [9] and it is particularly difficult in real devices. For this reason, the APT measurements of microelectronic materials are usually performed on thin films [10,11] or dedicated structure [12–18] and very few papers concern APT analysis of real transistors [19–21].

Focused ion beam (FIB) is widely used to fabricate specimens for APT from multilayer films and different authors [22–25] proposed procedures for specimen preparations based on lift-out by FIB.

In this paper, different lift-out methods have been used to analyze by APT real transistors and their applicability will be discussed. A special procedure of the specimen preparation for APT is proposed to position a transistor near to the tip apex by selective FIB lift-out and it has been used to analyze a sub-30 nm transistor from a static random access memory (SRAM) device. This analysis of the SRAM transistor gate by APT allows to characterize the formation of Ni silicides in real devices and thus to look at the effect of the confinement on the silicide reaction. The dopant distribution, metal gate composition and high-k dielectrics microstructure has also been determined from the APT analysis of the gate stack.

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2. Experimental procedures

The samples examined in this work were 0.15 and 0.3 μm^2 SRAM unit cell, formed respectively by 45 and sub-30 nm transistor fabricated with the standard process flow of 300 mm production wafers.

The analyzed transistors were long gate length n-type MOSFETs, consisting of a silicided poly-Si gate, a high-k oxide gate capped by a metal layer (TiN), and the Si substrate with source/drain extension and halo regions. The transistor fabrication has been performed by following standard gate-first procedure: after B atoms were implanted into the channel region, the Hf-based gate-oxide film, metal layer and P-doped poly-Si gate were formed. The sample was then patterned and etched by conventional lithography and dry etching. Dopant atoms were implanted for the source/drain extension and a spike annealing at 1065 °C was carried out to activate the implanted dopants. Finally conventional Ni silicide contacts have been created and the whole gate has been covered by a passivation layer before the deposition of the metal interconnections.

The FIB system used in these experiments was a Helios dual-beam equipped with a micromanipulator and by a gas injection system (GIS) for platinum deposition. The APT analyses were carried out in a LEAP 3000X HR instrument. The laser pulsing rate was kept at 100 kHz and the detection rate at 0.002 event/pulse by increasing the applied voltage. The specimen temperature and the laser energies were set between 20 and 50 K and between 0.3 and 0.6 nJ, respectively. Data reconstruction was done with the commercial IVAS software.

3. Methods

3.1. State of the art and purpose of this work

Several FIB-based methods have been developed to produce atom probe specimens from bulk materials and multilayered thin films. These techniques are similar to TEM sample preparation with a FIB, except that the sample extraction and subsequent mounting to a sample holder is designed to create the thin needle corresponding to the optimal geometry for atom-probe analysis. The goal of specimen preparation for the atom probe is to produce a specimen with an end radius of less than 100 nm on a smooth shank angle. The apex region of the specimen should have a uniform cross section without any grooves or protrusions. It is also important that the method used to prepare the specimen do not introduce any artifacts or change in the microstructure and/or the solute distribution. This procedure involves several steps [23,25]: (1) surface protection by Pt in situ deposition and definition of the region of interest on Si wafer via FIB milling; (2) extraction of the sample with an in situ micromanipulator; mounting of the extracted sample to a doped Si posts array that is designed to accommodate atom-probe specimens; (3) FIB sharpening of the extracted sample to a needle-shaped geometry using annular milling; (4) tip cleaning by low ion energy beam to remove most of the Ga damage and the Pt cap layer [26].

This classical top-down specimen preparation method works for simple specimen like bulk materials or thin layers, but in certain cases it results inadequate for complex structures like microelectronic devices that require very fine sample preparation.

The microelectronics industry widely uses FIB-machines for TEM-samples preparation at specific region of interest and has developed this technique in terms of reliability and time to result. The purpose of sequent paragraphs is to demonstrate that similar techniques can be employed for APT sample preparation taking into account to the already mentioned specificities of APT samples.

Fig. 1a shows a SRAM device that has been milled by FIB to isolate a thin slice from the surrounding material. The tungsten contact plugs (labeled C in Fig. 1), that connect the first metal layer with the source, drain and gate contacts of the transistors, and the seven levels of metal interconnection appear with a bright contrast (Fig. 1a and b). The transistors located between two W plugs are not directly visible in this slice because the cut is between two gate lines (Fig. 1c). However it is easy to distinguish the p and n type active lines separated by shallow trench insolation (STI) and thus to localize these positions. Fig. 1c is a plan view of the lowest SRAM levels, in which the poly-Si gates (horizontal lines) and the W contacts (white dots) are visible. Each vertical W contact line identifies an active zone.

Even though APT analysis has the capability to provide information on the whole SRAM device, the area of greater interest is the transistors level, because of its crucial importance for the devices and because of its complexity and its nanometric dimensions can hardly be characterized by conventional techniques. This part of the device is constituted by the active silicon with dopant implants and silicide contacts, and by the part of the gate located above the gate poly silicon. As shown by the white circle in Fig. 1, the tip has to be prepared at the intersection between active and gate zone by using the tungsten plugs as markers. Indeed these tungsten plugs form a periodic grid with strong bright contrast that it is clearly visible in standard SEM images. In the next paragraphs, several techniques, developed to extract a sample from SRAM devices and to realize a tip for APT analysis, are proposed and discussed.

3.2. Top down and backside methods

The first method is a simple adaptation of the classical procedure, usually called *top-down* method. The first concern in applying this procedure on real devices is the considerable depth, about 5 μm, at which transistor layer is buried under several metal/oxides layers. For this reason, it is preferable to extract a ~1 μm thick lamella (Fig. 2a) instead of the usual triangular wedge that is too big to be easily milled and manipulated by micromanipulator. The extracted lamella is mounted onto a post from a posts array (Fig. 2b) and then sharpened by FIB annular milling (Fig. 2c). The resulting tip presents a series of undesired nano-tips due to different milling rate of materials constituting the transistors. In particular, such nano-tips are formed by tungsten, a material harder to erode by ion beam than silicon. The effect of such unavoidable parasite tips is the modification of the electrical field around the tip during the analysis that dramatically affects the measurements.

Even though it is difficult to analyze transistors with this method, it can be employed successfully to analyze the W plug. Indeed, thanks to the low W erosion rate, a tip apex can be formed preferentially in correspondence to a W plug and takes the desired smooth shape.

To avoid the parasitic formation of W tip during tip preparation in correspondence of a transistor, an alternative way to the classical *top down* method is the *backside* approach in which the tip is fabricated after a 180° specimen rotation (Fig. 2d–h). This method, already employed for the study of thin films [27], allows the tip apex fabrication directly in the active Si zone free from metal lines and plugs as shown in Fig. 2h. The key step in this preparation method, i.e. the specimen rotation, is ensured by a special holder (Fig. 2e) equipped by a horizontal needle rotating around its axis. Once the sample is welded on the needle holder by platinum deposition, it is preferable to rotate it of 90° in order to remove the excess of material and to create a wedge like shape to ensure a better welding on the post after complete 180° rotation (Fig. 2f). The final annular milling is now executable on the silicon substrate and results in a smooth and protrusion free tip apex located in the silicon substrate (Fig. 2g).

This preparation method is potentially very effective, but with our samples it presents fundamental issues such as an increase