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Ultrathin epitaxial Ni-silicide contacts on (100) Si and SiGe: Structural and electrical investigations

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ABSTRACT

The formation of epitaxial $NiSi_2$ and NiSiGe layers is investigated. On Si(100) epitaxial $NiSi_2$ is obtained at $T > 400$ °C with a Ni layer thickness below 3 nm, while polycrystalline NiSi layer is produced with a 5 nm thick Ni layer. With increasing silicidation temperature, epitaxial $NiSi_2$ layers show a higher single crystalline quality, a lower resistivity and a lower Schottky barrier height to electrons. We highlight the extremely low contact resistivity of epitaxial $NiSi_2$, which is about one order of magnitude lower than that of NiSi on both, As and B doped SOI. Epitaxial NiSiGe is also obtained on (100) SiGe employing an Al interlayer mediated epitaxy growth method. The Al atoms from the original 3 nm interlayer diffused towards the surface during annealing. The incorporation of some Al increases the transition temperature from the Ni-rich germano-silicide phase to the mono-germano-silicide phase. The formed epitaxial $NiSi_{0.7}Ge_{0.3}$ shows an orthorhombic structure with a (101) base plane rotated by 45° with respect to the (100) $Si_{0.7}Ge_{0.3}$ substrate.

1. Introduction

As the scaling of device dimensions continues, new materials like SiGe for high hole mobility channels, thin silicides for low contact resistivity source/drain (S/D) regions, are required. According to the International Technology Roadmap for Semiconductors (ITRS) [1], for the 18 nm technology node, the silicide layer thickness should not exceed 12 nm and its specific contact resistivity on highly doped S/D should be smaller than $8 \times 10^{-8}\,\Omega\,cm^2$. Reducing the contact resistance is a big challenge in achieving small S/D resistance, as the silicide contact resistance contributes more than 80% to the total S/D series resistance at 18 nm node, according to MASTAR simulations [1].

Among the various transition metal silicides, NiSi is the most suitable material. However, its low thermal stability of the polycrystalline phase lead to rough interfaces and contact edges, consequently may give rise to a large variability of the performance of nano devices. Platinum (Pt)-incorporation into Ni-silicide, to form $Ni_{1-x}Pt_xSi$, improves the thermal stability and lowers the contact resistivity [2,3]. However, a better approach to improve the thermal stability and especially the interface quality is to employ epitaxial silicides. Nickel disilicide ($NiSi_2$) is one of the promising candidate materials due to its small lattice mismatch, only −0.4%, with respect to Si. Epitaxial $NiSi_2$ (epi-$NiSi_2$) layers on Si(001) can be easily formed by solid-phase reaction of Ni with Si at temperatures >700 °C. However, thick $NiSi_2$ layers, formed by direct annealing of a thick Ni layer on Si, often exhibit a discontinuous and inhomogeneous morphology induced by the formation of {111} facets at the $NiSi_2$/Si(100) interface. High quality epi-$NiSi_2$ layers can only be formed with a Ni thickness in the range of 1–3 nm [4,5].

Uniform contacts on SiGe are much more difficult to form than on pure Si. In the ternary (Ni,Si,Ge) systems, the phase reactions and morphological transformations are more complex [6]. Island structures and Ge segregation have been observed after high-temperature treatments [7,8]. The different enthalpy of formation of NiSi ($-45\ kJ\ mol^{-1}$) from that of NiGe ($-32\ kJ\ mol^{-1}$) causes the failure of forming highly uniform $NiSi_{1-x}Ge_x$ layers [9]. Ge is incorporated in the Ni ($Si_{1-x}Ge_x$) phase when formed at lower temperatures, while at higher temperatures Ge diffuses out, allowing a minimization of the Gibbs free energy by the formation of thermodynamically stable phases like NiSi [10]. The epitaxial growth of ternary silicides is difficult due to the complicated reactions as mentioned above and different crystal structures, orthorhombic $NiSi_{1-x}Ge_x$ and cubic $Si_{1-x}Ge_x$.

In this paper, we present results on the formation of ultra-thin Ni silicide layers on SOI and NiSiGe on SiGe. Special emphasis is placed on the epitaxial $NiSi_2$ and NiSiGe layers. The structural and electrical properties of these epitaxial layers will be presented.

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2. Ultra-thin Ni silicide formation on Si

Bulk Si(100) and SOI (100) wafers with a top Si thickness of 88 nm were used as starting materials. The thickness of the buried oxide (BOX) is 145 nm. Three different metal layers were used for silicidation: 3 nm Ni, 5 nm Ni and 3 to 5 nm Ni with 1 nm Pt interlayer deposited by electron-beam evaporation, as shown in Fig. 1. The samples were annealed by rapid thermal processing (RTP) at different temperatures for 10 s to form the silicide layers. The residual unreacted metal was chemically etched selectively.

Fig. 2 displays the silicidation temperature windows for forming the lowest resistivity silicides on SOI using the metal layers shown in Fig. 1. Monosilicide (NiSi) layers were formed with 5 nm Ni at 350 °C < T < 600 °C with the minimum sheet resistance of 15 Ω/square. With 1 nm Pt interlayer and 5 nm Ni, $Ni_{1-x}Pt_xSi$ layers were formed from 400 °C to 700 °C with a sheet resistance of ~30 Ω/square. The incorporation of Pt enlarges the thermal stability of $Ni_{1-x}Pt_xSi$ by 100 °C compared with NiSi layers, but decreases if the Ni thickness decreases to 3 nm.

Fig. 3 shows cross-section transmission electron microscopy (XTEM) images of silicide layers formed at 500 °C using 5 nm Ni and 1 nm Pt/5 nm Ni on SOI. All silicides have a thickness of about 11 nm. The $Ni_{1-x}Pt_xSi$ layer presents a smoother interface to the underlying SOI layer than NiSi.

With only 3 nm Ni a much wider formation temperature window and a thermal stability up to 950 °C are observed. In this case an epitaxial $NiSi_2$ layer was formed, as will be discussed in the following. The XTEM images of Fig. 4 indeed show an epitaxial $NiSi_2$ layer (epi-$NiSi_2$) formed at T > 400 °C, in agreement with the results reported by Tung et al. [4,5]. The crystalline and interface quality of the epi-$NiSi_2$ layers formed on SOI improves at higher silicidation temperatures: at 500 °C only few pyramids with wedge-shaped (111) facets at the epi-$NiSi_2$/Si interface are observed but at T > 850 °C high quality single crystalline $NiSi_2$ layers with sharp epi-interface were obtained. The resistivity is 16.5 μΩ cm, for NiSi; 33.0 μΩ cm, for $Ni_{1-x}Pt_xSi$; and for epi-$NiSi_2$, 45.0 μΩ cm.

Grazing incidence X-ray diffraction (GI-XRD) of NiSi formed with 3 and 5 nm Ni at various temperatures is presented in Fig. 5. Only NiSi phase peaks are found for the 5 nm Ni case, indicating a polycrystalline NiSi layer. For the Ni silicide layer formed with 3 nm Ni at 450 °C we found only the peaks from the Si substrate and no NiSi peaks were observed. Because the lattice mismatch of $NiSi_2$ to Si amounts to only −0.4% it is hard to distinguish the $NiSi_2$ signal from the Si substrate in the XRD measurements. To reveal the crystallinity of the $NiSi_2$ layers formed with 3 nm Ni we employed Rutherford backscattering spectrometry/channeling (RBS/C). Fig. 6 shows the RBS/C spectra for the $NiSi_2$ layers processed at different temperatures. He ion channeling in the $NiSi_2$ layers improves with increasing silicidation temperature

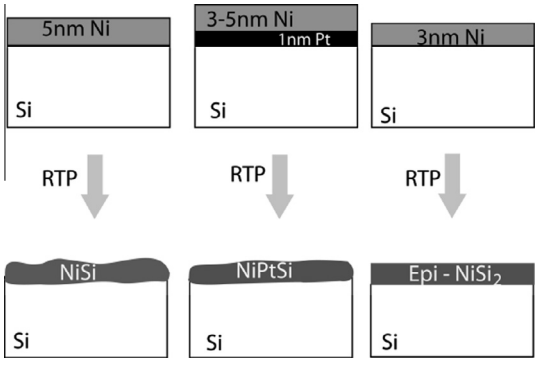

Fig. 1. Ni silicidation processes with different Ni starting layers.

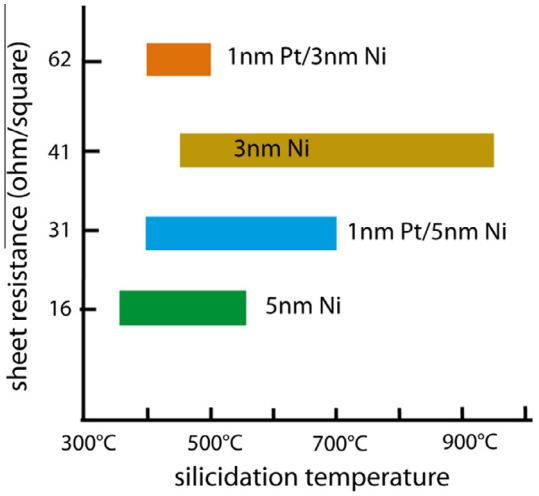

Fig. 2. Silicidation temperature windows for forming silicide layers with the lowest resistivity.

indicating the improvement of the single crystalline quality with increasing temperature. Furthermore, the RBS results confirm the silicide layers formed at T > 400 °C are in $NiSi_2$ phase.

3. Schottky barrier height and contact resistance characterization of Ni silicides on Si

The Schottky barrier heights (SBHs) of ultra thin silicides were measured with diode structures formed on n-Si(100) bulk substrates.

Fig. 7 shows typical I–V characteristics of Schottky diodes measured at room temperature (RT) for different silicides on n-Si(100). The NiSi and $Ni_{1-x}Pt_xSi$ layers were fabricated using 5 nm Ni and 1 nm Pt/5 nm Ni at 500 °C, respectively, while the epi-$NiSi_2$ layers were formed with 3 nm pure Ni at various temperatures. A comparison of the reverse currents in Fig. 7 indicates that $Ni_{1-x}Pt_xSi$ has a higher SBH than NiSi. For $NiSi_2$ layers, the SBH decreases with increasing silicidation temperature. We assume that the SBH of epitaxial $NiSi_2$/Si contacts is strongly dependent on interface quality, specifically on the density of {111} facets at the interface. A correlation between the decreasing SBH of n-type contacts and the density of {111} facets is observed. Consistently, a uniform $NiSi_2$ layer without facets shows the lowest SBH [11].

The measured SBH and the ideality factor "n" for different silicides formed on n-Si(100) are summarized in Fig. 8. $Ni_{1-x}Pt_xSi$ has the highest SBH of 0.76 eV. As expected from the I–V characteristics in Fig. 7, the SBH of epi-$NiSi_2$ layer decreases from 0.49 eV to 0.35 eV when the silicidation temperature is raised from 400 °C to 850 °C. All silicide contacts show ideal "n" factors with values ranging from 1.1 to 1.07. The "n" value of epitaxial $NiSi_2$ layers decrease slightly from 1.09 to 1.06 by increasing the silicidation temperature from 400 °C to 850 °C.

The contact resistivities of various silicides to SOI were measured using transmission line model (TLM) structures. SOI substrates with a top Si thickness of 88 nm were first implanted with As^+ at an energy of 30 keV or B^+ at 6 keV to a dose of 2×10^{15} cm^{-2}, and then annealed at 1000 °C for 1 min in order to produce uniformly doped SOI layers. After patterning an oxide layer, deposited by low pressure chemical vapor deposition, self-aligned silicidation was performed to form TLM structures with spacing distances ranging from 5 μm to 150 μm. Al contacts were deposited on the silicide. The contact resistance was measured at RT.