Microelectronic Engineering 107 (2013) 196–199

Contents lists available at SciVerse ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Silicided Au/Ni bilayer on p-type [001] silicon for low contact resistance metallization schemes

Paolo Badalà [a,*], Antonello Santangelo [a], Giovanna Pellegrino [b], Alessandra Alberti [b]

[a] STMicroelectronics, Zona Industriale Stradale Primosole 50, Catania 95121, Italy
[b] CNR-IMM, Zona Industriale Strada VIII 5, Catania 95121, Italy

ARTICLE INFO

Article history:
Available online 13 October 2012

Keywords:
Nickel silicide
Specific contact resistance
Backside metallization
Trans-rotational structures

ABSTRACT

Rear contact terminals of integrated circuits have to satisfy electrical and mechanical requirements, such as low specific contact resistance, good adhesion to the substrate and good solderability with external elements. A new metallization scheme, made of sputtered Ni and Au layers, with the addition of a process step needed to ensure nickel silicide formation at low temperature, has been proposed for p-type silicon substrates and investigated in this work. Its electrical and structural properties have been compared with conventional Cr/Ni/Au and Ti/Ni/Au contacts, showing lower specific contact resistance values (ρ_c), an ohmic behaviour in the explored range of resistivity (i.e. 3 mΩ cm < ρ < 18 mΩ cm) despite of the rectifying one of conventional materials, better adhesion with the substrate and limited consumption of nickel and silicon during the reaction process. The proposed metallization scheme provides an effective solution to meet both electrical and mechanical requirements with a single material, with a consequent reduction of logistic and economic effort to realize integrated circuits.

1. Introduction

Backside metallization on Si wafers has to guarantee very low contact resistance between metal and silicon, good adhesion to the substrate and soldering on package. This is important in the field of high power discrete vertical devices, i.e. P-channel MOS (Power Metal Oxide Semiconductor devices) and IGBT (Insulated Gate Bipolar Transistor), or in the domain of ICs (Integrated Circuits), where parasitic currents must be collected from the backside contacts. A well known way to reduce metal/semiconductor contact resistance is incorporating in the substrate as much p-type acceptor as possible, in order to promote the tunnelling through the Schottky barrier. This way can be pursued down to few mΩ cm, but high doped substrate can make the growth of thin epi-layer difficult, or consume it during the usual annealing, due to the high concentration gradient. To mitigate the contact resistance issue, it is useful to adopt a first metal layer in direct contact with the silicon substrate, which exhibits the lowest barrier height on p-type silicon. For example, Au and Pt could represent a suitable choice, but their adhesion to silicon is normally quite poor. Therefore a compromise between adhesion and barrier height is mandatory. The uppermost metallic layer deposited on the backside should guarantee a good wettability by the usual low melting alloy (e.g. PbSn, SnAgCu), used to solder the silicon dice on the package.

Because of the difficulty to meet all these needs with a single material, backside metallization is often made up of multilayer structures including different metal layers, where each one is intended to satisfy a specific requirement, leading to complex and unproductive processes. A typical multilayer structure on p-type silicon substrates is made by the sequential deposition of Cr, Ni and Au layers. Nevertheless, metal peeling issues sometimes occur for high doped substrates (e.g. >2 × 10^{19} B/cm^3), due to weak adhesion between Cr and Si. Furthermore, for low doped substrates (i.e. 3 × 10^{18} ÷ 8 × 10^{18} B/cm^3), the contact is found to be rectifying, due to a Schottky diode formed at the semiconductor–metal junction. A new metallization scheme, made of sputtered Ni and Au layers, with the addition of a process step needed to ensure nickel silicide formation at low temperature (<300 °C), has been proposed and investigated to solve these issues.

2. Experimental setup

P-type [001] silicon substrates with resistivity in the range from 3 to 20 mΩ cm have been selected. A thin SiO_2 layer was grown on wafer surface, preceding boron implantation at 30 keV and a dose of 5e15/cm^2, in order to reduce the contribution of the front metallization to contact resistance. The implanted boron was subsequently activated at 1100 °C for 30 s. A Spreading Resistance Profile (SRP)

* Corresponding author.
E-mail address: paolo.badala@st.com (P. Badalà).

0167-9317/$ - see front matter © 2012 Elsevier B.V. All rights reserved.
http://dx.doi.org/10.1016/j.mee.2012.09.009

analysis was performed to evaluate the increasing of doping concentration near the surface, revealing $1 \times 10^{20}/cm^3$. Such a concentration is equivalent to a resistivity of $1 \times 10^{-3}\ \Omega$ cm, and to a specific contact resistance of aluminium to silicon of $1 \times 10^{-7}\ \Omega\ cm^2$ [1]. On the basis of these results, after thermal oxide removal, a layer of AlSiCu of thickness 3.2 μm was deposited by sputtering on the front of each wafer. Wafer thickness was then reduced to 150 μm by mechanical grinding and chemical etching, with polish finishing and an HF final step, in order to reduce the contribution of the substrate to contact resistance. A double layer of Ni (500 nm) and Au (50 nm) has then been deposited on the backside of the wafers, by sputtering in Ar ambient at a base pressure of 1×10^{-3} mbar. Two reaction processes have been studied. In the first case, nickel silicide formation has been obtained *in situ*, by sputter etching the surface for 180 s before metal deposition, in the same Physical Vapour Deposition (PVD) equipment, without vacuum interruption. In the second one, the reaction has been performed *ex-situ*, by annealing the sample at 200 °C for 10 s in nitrogen ambient, between Ni and Au topmost layer deposition. Even in the second case, Ni deposition has been preceded by a sputter etching step of 30 s, to remove residual surface contaminations. Two more metallization schemes – Cr/Ni/Au (100/400/50 nm) and Ti/Ni/Au (100/400/50 nm) – have been analysed and compared to silicide contacts, since they are commonly used on p-type and n-type Si respectively. *J–V* characteristics of test structures – dies of area 9 mm^2, assembled on a package as shown in Fig. 1 – have been measured by forcing current from −100 to 100 A by an automatic tool (TESEC 8881-TT/A). Specific contact resistance of backside metallization has then been obtained as $\rho_c^{back} = R_{tot} \times A_{die} - \rho_{sub} \times th_{sub}$, where R_{tot}, that represents the resistance of the whole stack to current flowing, has been calculated by fitting the *J–V* curves in the origin's neighbourhood and the contribution of front metallization to contact resistance has been neglected, on the basis of previous considerations [1]. Moreover ρ_{sub} is the substrate's resistivity, measured as $\rho_{sub} = R_s \times th_{sub}$ (where R_S is the substrate's sheet resistance, measured by *Four Point Probe* (FPP) method), and die size (A_{die}) and substrate's thickness (th_{sub}) have been previously measured. In order to evaluate any possible relationships with the electrical properties, the structure of silicided samples has been investigated by means of plan-view and cross-sectional Transmission Electron Microscopy (TEM) – using a JEOL-JEM microscope working at 200 keV – and by X-ray Diffraction (XRD) analyses, using a Bruker AXS D8 DISCOVER diffractometer working with a Cu-Kα source and a thin film attachment.

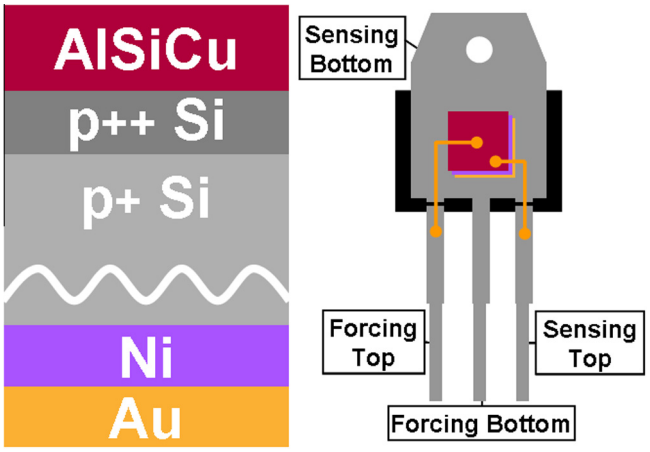

Fig. 1. Not in scale schematic drawing of experimental configuration used to measure specific contact resistance of backside metallization. On the left side is reported the cross section of the test structure, while right side shows the assembled die.

3. Results and discussion

J–V curves reported in Fig. 2(a) show, in the resistivity range from 10 to 14 mΩ cm, that the Ni/Au metallizations, both *in situ* and *ex-situ* reacted, are ohmic and less resistive than the Cr/Ni/Au and Ti/Ni/Au ones, which have instead a rectifying behaviour. Similar characteristics are found for Ni, Cr and Ti samples in the resistivity range from 14 to 20 mΩ cm, as shown in the *J–V* curves of Fig. 2(b).

The specific contact resistance values (as extracted by the *J–V* curves) versus the substrate resistivity are shown in Fig. 3. As expected on the basis of the literature [2,3], Ti/Ni/Au samples exhibit the highest contact resistance in the whole explored range, because of the high Schottky Barrier of titanium on p-type silicon. Ni/Au contacts, both *in situ* and *ex-situ* reacted, show contact resistance values lower than those of conventional Cr/Ni/Au metallizations, for substrate's resistivity range from 10 to 20 mΩ cm, and comparable to them for resistivity less than 5 mΩ cm, when a tunnelling process of the carriers through the electrical barrier becomes dominant. The Cr/Ni/Au is randomly affected by peeling, for lower resistivity substrates, and by a rectifying behaviour, on higher resistivity substrates. When contact resistance of metal to semiconductor rises so that it is not negligible compared to device's

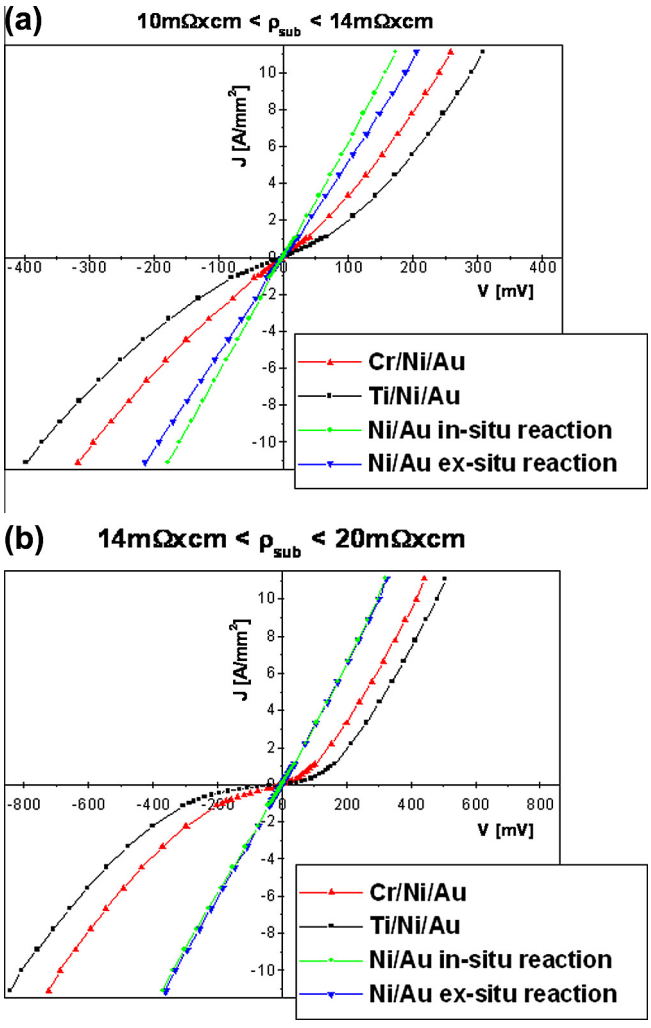

Fig. 2. *J–V* curves of test structures for substrate's resistivity values between 10 and 14 mΩ cm (a) and between 14 and 20 mΩ cm (b). The Ni/Au metallizations are ohmic and less resistive than the Cr/Ni/Au and Ti/Ni/Au ones, which exhibit a rectifying behaviour.