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Alignment verification for electron beam lithography

Stephen Thoms [a,*], Douglas S. Macintyre [a], Kevin E. Docherty [b], John M.R. Weaver [a]

[a] School of Engineering, University of Glasgow, Glasgow G12 8QQ, UK
[b] Kelvin Nanotechnology Ltd., Glasgow G12 8LT, UK

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ABSTRACT

Alignment between lithography layers is essential for device fabrication. A minor defect in a single marker can lead to incorrect alignment and this can be the source of wafer reworks. In this paper we show that this can be prevented by using extra alignment markers to check the alignment during patterning, rather than inspecting vernier patterns after the exposure is completed. Accurate vernier patterns can often only be read after pattern transfer has been carried out. We also show that by using a Penrose tile as a marker it is possible to locate the marker to about 1 nm without fully exposing the resist. This means that the marker can be reused with full accuracy, thus improving the layer to layer alignment accuracy. Lithography tool noise limits the process.

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1. Introduction

Alignment of patterns defined by electron beam lithography is often required to sub 10 nm accuracy [1], for example when using double patterning [2] or fabricating photonic [3] or diffractive optic elements [4]. The use of this degree of accuracy has moved from fabricating occasional novel devices to a routine requirement, and thus the reliability of such alignment is of increasing importance. As with all fabrication steps it is important to have test structures [5] that can be used to monitor the quality of the lithography step in a non-destructive manner, ideally giving feedback immediately after the step has been carried out and before further processing. Vernier test structures, which are used to compare the developed resist with the marker level on the wafer and can be read with an optical microscope immediately after development, are often used. Unfortunately these cannot give the desired level of accuracy; the typical precision and accuracy of such verniers are around 50 nm. Usually the only way to ascertain if the alignment has been carried out satisfactorily is to carry out pattern transfer after resist development, and then inspect the wafer using a scanning electron microscope. As well as being time consuming, this has the serious drawback that faults are discovered too late. If there is an error, then the wafer must be scrapped and the only saving is that of avoiding unnecessary fabrication steps.

Fresh alignment markers need to be used for each level because of the high exposure dose generally given to each marker during the exposure process [3]. Alignment errors generally arise from either misshaped or misplaced markers, but also arise from the fact that different markers are used for each lithography level. This is because when a different set of markers is used there is an extra level of indirection in the alignment process. In other words, the errors arise not only from the alignment process itself, but also from the errors in position between the two sets of markers. This latter error may only be of the order of a few nanometres, but is important in the context of sub 10 nm alignment.

Penrose tiles have been shown to have many desirable properties for electron beam markers when using image correlation as the mark locate method [6]. One property which was predicted but not previously explored is the ability to reduce the applied dose during marker search so as to avoid exposing the resist. This paper shows that this is possible without losing marker search accuracy. It also demonstrates that collecting an image of a Penrose tile during exposure can be an effective alternative to a vernier test structure, and can be used to obtain sub 10 nm alignment information in a non-destructive and rapid manner.

2. Theory

There are a number of important considerations when choosing a marker design for correlation search. The ideal marker should have a sharply peaked autocorrelation, which from the Wiener–Khintchine theorem is equal to the Fourier transform of the power spectral density (PSD). This means that the PSD itself is broad, implying the presence of all frequencies in the Fourier transform. A Penrose tile satisfies this requirement because of its aperiodic nature.

* Corresponding author. Tel.: +44 141 330 5656.
E-mail address: stephen.thoms@glasgow.ac.uk (S. Thoms).

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In addition the autocorrelation should be well behaved under the condition of undersampling. This is important when seeking to avoid fully exposing the resist during marker search. This requires a reduction in the exposure dose imparted to the resist during image capture, while maintaining the signal to noise ratio. A constant signal to noise ratio is obtained by maintaining both the pixel dwell time during image capture, and also the same number of pixels. Under these circumstances the only way in which the average dose can be reduced is to increase the pixel spacing, which results in undersampling. Patterns with edges aligned to the horizontal and vertical axis, such as squares and Barker codes, behave badly under conditions of undersampling, whereas a Penrose tile maintains the sharpness of its autocorrelation function as the pixel spacing improves, as is illustrated in Fig. 1. The autocorrelations are all normalised to enable better comparison of the central peaks. The Sierpinsky carpet pattern for alignment can give a sharp autocorrelation peak when undersampled, but not for all pixels sizes, as illustrated in Fig. 1. Even when it does give a sharp autocorrelation peak, it is not as sharp as that obtained using the Penrose tile pattern, which remains sharp for all pixel spacings.

It may also be necessary to defocus the beam in order to prevent exposure of an array of dots during image collection. The effect of a moderate defocus on the spot size is to increase the Gaussian size of the beam. The effect on the correlation function is simply to convolve it with the Gaussian beam profile, which leads to a Gaussian peak at the centre of the correlation. This broadens as the defocus increases. Even for zero defocus the beam profile is approximately Gaussian, so its centre can be always be found by fitting to a Gaussian.

3. Methodology

All electron beam lithography exposures were carried out using a Vistec VB6 tool operated at 100 kV. The resist used in all cases was a bilayer of PMMA (polymethylmethacrylate) with molecular weights of 85 and 360 k; the developer used was a 2.5:1 mixture of IPA:MIBK (isopropyl alcohol:methyl isobutyl ketone), which results in a resist sensitivity of 366 μC/cm^2 for large features on a silicon substrate.

To find the size of the image required to avoid fully exposing PMMA, a series of images of PMMA on silicon were collected using the VB6 with a beam defocused to between 30 and 150 nm, and a capture rate suitable for correlation mark location. Each image was a 100 pixel square and used the same scan rate, but had increasing image size (2, 4, 5, 8, 10, 15, 20 μm), thus decreasing the applied dose. The size, L, for which the resist was not fully exposed was determined.

A second test was designed to compare two different methods of monitoring the alignment error between lithography levels. This test was carried out on a 3″ silicon wafer with multiple 1 cm square cells. Each cell contained local alignment markers, and an array of alignment test patterns. The test pattern consisted of a Penrose tile marker larger than L adjacent to the first level of a conventional vernier pattern with 2 nm resolution. The vernier pattern was designed to be read using a scanning electron microscope. After development a gold liftoff process (10 nm Ti/50 nm Au) was carried out. A second lithography level was aligned to the first level in which the second level of the verniers was written and images of the Penrose markers were collected. Again, gold liftoff was carried out.

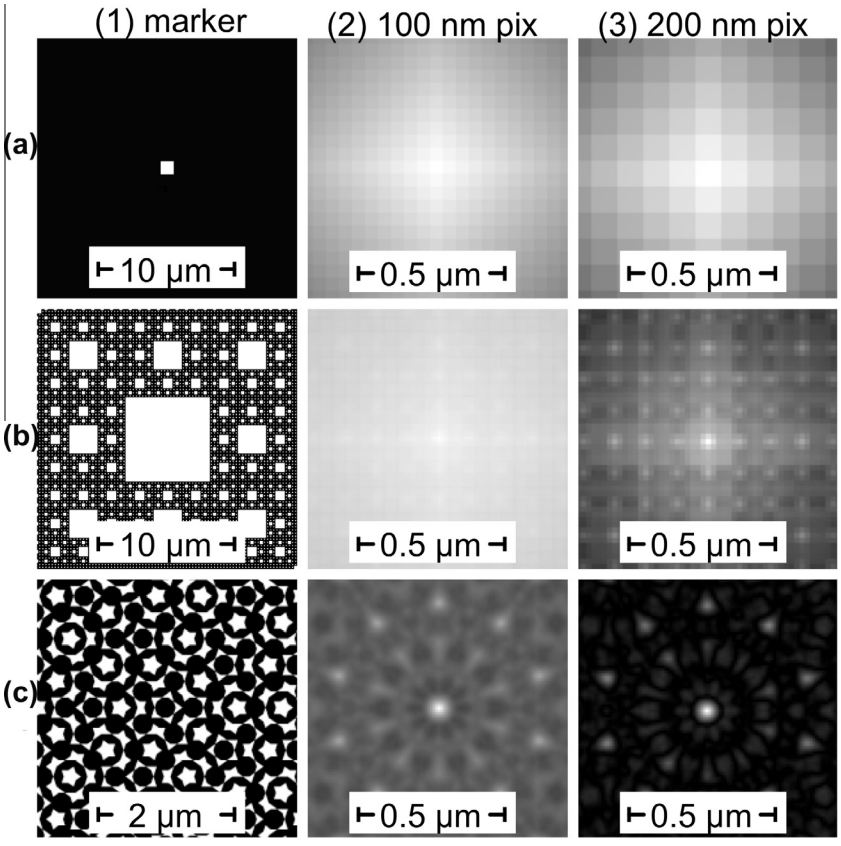

Fig. 1. Three different marker designs and their autocorrelation using different amounts of undersampling. (a) Shows a 2 μm square marker, (b) shows a Sierpinsky carpet with minimum rectangle size of 80 nm, and (c) shows a Penrose tile with minimum feature sizes around 100 nm. The centre of the autocorrelations are all shown with the same normalised brightness scale.

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