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Specific features of silicon surface region fluorination by RIE in r.f. CF_4 plasma – A novel method for improving the electrical properties of thin PECVD silicon oxide films

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ABSTRACT

In this study, we compare a previously reported method of improving the electro-physical properties of silicon dioxide (SiO_2), which uses silicon substrate fluorination in CF_4 in a Plasma Enhanced Chemical Vapor Deposition (PECVD) reactor prior to oxide deposition, with our proposed method of fluorination in CF_4 in a classical Reactive Ion Etching (RIE) reactor.

The careful analysis of the location and behavior of fluorine profile during PECVD gate oxide deposition was done by means of Ultra Low Energy-Secondary Ion Mass Spectroscopy (ULE-SIMS). The observed effects were used to determine changes in the electrical properties of the dielectric layers from the two fluorination methods being studied.

The results showed that, in general, fluorination in a RIE reactor is superior to fluorination in a PECVD reactor. The advantage of the former technique is that most of the electro-physical properties of the resulting Metal–Oxide-Semiconductor (MOS) structures are significantly better. The change in the properties of gate stacks was shown to be fluorine concentration dependent, which can be controlled by the parameters of the RIE (e.g., by r.f. power supplied to the discharge). However, this study concluded that the fluorine profile parameters cannot be controlled independently.

1. Introduction

As semiconductor devices are scaled down to realize higher-performance Ultra-Large Scale Intergration (ULSI) devices, the reliability of gate-oxide films becomes one of the most important issues. The downscaling of gate oxide thickness improves current driving capabilities and reduces short-channel effects. However, ultrathin oxide films exhibit many serious reliability problems, such as time-dependent dielectric breakdown, interface-state generation and charge trapping (e.g. [3]). The fluorination of silicon substrates has been investigated as a possible solution for these problems [1–9]. Many of the properties of silicon dioxide (SiO_2) layers fabricated on fluorinated substrates have already been studied. For example, such oxides have been found to be more resistant to ionizing radiation [4], Fowler–Nordheim (F–N) tunneling injection stress [3–5] and channel hot electron stress [6]. A dramatic reduction of both the hole-trapping probability and interface-trap generation in fluorinated samples under avalanche hole injection conditions has also been reported [8]. In [9], it was shown that the degree of improvement when using fluorinated substrates is a function of fluorine concentration, which has led to efforts to increase the concentration of fluorine in silicon dioxide films.

Thus far, a number of methods for fluorinated gate oxide fabrication have been proposed, which include immersing Si wafer in a HF solution without a D.I. water rinse prior to oxidation [1], ion implantation of fluorine atoms into poly-Si gates followed by a high temperature drive-in [4] or rapid thermal processing in O_2 with diluted NF_3 [9].

As shown in [1], CF_4 plasma pretreated silicon substrate followed by PECVD oxide can be an attractive method for fabricating high quality thin (fluorinated) gate silicon dioxides. In this work, we demonstrate that fluorination in CF_4 plasma generally improves all of the electrical parameters of gate oxides obtained by PECVD, e.g., charge to breakdown Q_{bd} distribution and threshold voltage – *U*th values.

Our recent studies have shown that RIE processes in CF_4 plasma are good methods for incorporating high concentrations of fluorine ions (even on the order of 10^{19} cm^{-3}) into silicon surfaces and can also be used for fluorination [10]. It was also shown in [10] that fluorine is not stable on silicon surfaces that have been exposed to very high temperatures (on the order of 1000 °C); thus, fluorination cannot be used to improve the properties of layers fabricated under high temperature conditions. However, we also showed in

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[10] that fluorination by RIE, which allows for the incorporation of high concentrations of fluorine, significantly improves the electrical characteristics of MOS structures.

The aim of this study is to investigate RIE fluorination in more detail and compare it to previously reported method of fluorination by using CF_4 plasma in PECVD reactors [1]. In this study, we will also try to determine the relationship between fluorine in the silicon/oxide system during oxide layer formation by PECVD, the type of reactor used for fluorination and the effects on the electro-physical properties of MOS structures.

2. Experimental procedures

The complete list of most important processes performed in the course of this study is shown in Table 1. In this work, three types of semiconductor/dielectric structures were investigated and compared:

- PECVD silicon dioxide with no preceding pretreatments (reference sample);
- PECVD silicon dioxide deposited on a silicon substrate pretreated in CF_4 plasma (in a RIE reactor – samples nos. 1–3)
- PECVD silicon dioxide deposited on a silicon substrate pretreated in CF_4 plasma (in a PECVD reactor – sample no. 4);

The complete process flow is described in the following section. First, boron-doped, (1 0 0)-oriented silicon wafers with a resistivity of 4–10 Ωcm were cleaned using standard procedures (SC1 + SC2 + BHF) prior to oxide formation. Then, the silicon surface was covered with a 10 nm initial oxide that was deposited using PECVD at 300 °C. The role of the latter oxide was the protection of silicon substrates during plasma fluorination.

PECVD and RIE fluorination processes were performed in a conventional Oxford PlasmaLab system to implant fluorine atoms through the thin dielectric layer. The initial SiO_2 film was reactively etched in a RIE at room temperature by flowing 50 ml/min of CF_4 at 200 mTorr to achieve plasma discharge. The r.f. power used to generate plasma was set to 80, 120 and 160 W for each experiment.

In order to compare the efficiency of fluorination performed by RIE in CF_4 with previously described method, fluorination in CF_4 plasma by PECVD [1] was also performed. To obtain a reasonable comparison, fluorination by RIE was carried out at room temperature and PECVD was carried out at an elevated temperature (300 °C). This ensured optimal electro-physical properties for the respective processes. All other parameters of the PECVD and RIE processes (pressure, r.f. power and process time) were identical. Only the highest r.f. power was used in this experiment (160 W) since, as reported in [9], the largest improvement is expected from the highest fluorine concentration.

Due to increased temperatures in the reaction chamber and the presence of active fluorine (resulting from the breakdown of CF_4 particles in r.f. plasma), the initial oxide was also completely removed during fluorination by both processes, which was verified using ellipsometric measurements.

After fluorination, the final silicon dioxide layer was deposited by PECVD. The thickness of the final gate dielectric film was 13 nm. All ellipsometric measurements were determined by using Gaertner ellipsometer (λ = 632.8 nm).

The distribution and concentration of fluorine in the silicon/oxide system, with the exception of a reference system, were measured using ULE-SIMS. The SIMS measurements were conducted using a SAJW-05 instrument with a Balzers quadrupole-based mass analyzer (QMA-410). The apparatus was also equipped with a 06-350E Physical Electronics Ar^+ ion gun. The samples were sputtered with Ar^+ primary ions at 880 eV impact energy. The use of an ultra-low energy primary beam for sputtering helped to reduce atomic mixing and to produce profiles with high depth resolution. The ion beam, which was approximately 100 μm in diameter with a current of 70 nA, was rastered over a 2000 × 3000 μm area.

In order to use electrical characterization methods for the evaluation of the electro-physical properties of the obtained silicon/oxide systems, Metal–Oxide-Semiconductor (MOS) capacitors with gate dielectric layers were fabricated. Here, aluminum was used as the metal gate.

3. Results and discussion

3.1. SIMS characterization of fluorine content

It was established in [10] that the Reactive Ion Etching (RIE) process in fluorine plasma is a good method for incorporating fluorine into silicon substrates and fabricating oxide layers with high concentrations of fluorine atoms. These layers are very thin (about 1.5 nm) and have a maximum concentration of fluorine greater than 10^{19} cm^{-3}. Here, the concentration of fluorine atoms can be controlled by changing the RIE process parameters, e.g., by adjusting the r.f. power.

An example of the profile of the final PECVD oxide deposition on the RIE fluorinated substrates is presented in Fig. 1. One can easily see that a relatively narrow fluorine profile located very close to the silicon/oxide interface (only a few nanometers thick) can be obtained after the PECVD process. In fact, four regions can be structurally distinguished: the oxide, the fluorine-rich oxide, the fluorine-rich silicon and the silicon bulk (Fig. 1).

The comparison of the fluorine profile before and after the final PECVD oxide formation is presented in Fig. 2. It is important to note that PECVD carried out at 300 °C did not neither seriously affect the fluorine profile, nor did it result in high temperature annealing, where the fluorine is completely removed from the silicon surface region [10]. It can easily be seen that the fluorine peak has decreased by approximately half an order of magnitude, broadened and moved to some depth in the silicon dioxide layer. The first two effects can easily be attributed to thermal rediffusion processes

Table 1
Experiment matrix and plasma process parameters.

Sample	Reactive ion etching (RIE) in r.f. CF_4 plasma			PECVD silicon surface plasma pretreatment in r.f. CF_4				Final SiO_2 deposition in PECVD plasma			
	Flow of CF_4 [scan]	Pressure [mTorr]	r.f. Power [W]	Flow of CF_4 [scan]	Pressure [mTorr]	r.f. Power [W]	Temperature	Flows of gases [sccm]	Pressure [mTorr]	r.f. Power [W]	Temperature (°C)
1			80								
2	50	200	120			–		N_2O = 120			
3			160					SiH_4 = 70	600	10	300
4	–			50	200	160	300				
Reference	–					–					