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Invited paper

Phase Change Memory lifetime enhancement via online data swapping

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ABSTRACT

As DRAM technology is facing scalability limitations due to its excessive leakage power in nano-scale technologies, various non-volatile memory technologies have been emerged to replace it in memory hierarchy. Among these technologies, *Phase Change Memory* (PCM) is a promising technology for main memory due to its near-zero leakage power, higher density, non-volatility and soft error immunity. However, its major drawbacks, including high write energy and limited write endurance, have prevented its usage as a drop-in replacement of DRAM technology. In this paper, we propose a technique to swap data between memory lines with goal of reducing bit flips. The proposed swapping technique finds the best place to write a chunk of data among a limited set of lines to minimize number of bit flips. The proposed swapping operation works online i.e, does not require any data profiling. Moreover, it does not require major modifications of existing solutions and works only by the addition of a proposed circuitry. It is remarkable that, this technique is additive to various other architectures aiming at PCM lifetime enhancement. Experimental results carried out on a quad core CMP system show that the proposed technique prolongs PCM main memory lifetime by 48% which is achieved at the price of 1% and 2% overhead in read and write latencies respectively.

1. Introduction

High power consumption of DRAM-based memories along with their high susceptibility to high energy particle strikes (known as soft errors) have forced VLSI designers to find some replacements to use in modern multi-core chips. Emerging non-volatile technologies such as *Phase Change Memory* (PCM) have gained a lot of attention as ostensible replacements of DRAM technology in main memory [1–3]. Such vast attention is mainly due to PCM higher density, near-zero leakage power, non-volatility and comparable performance with DRAM [4]. The application of PCM in main memory reduces the power consumption, increases chip density, improves soft-error immunity [5,6] and even makes it more cost effective [7,5].

However, main drawbacks of PCM technology including limited write endurance, high write energy and write latency, have prevented it from being used as a drop-in replacement of DRAM technology [8,9]. Although PCM read operation is comparable with DRAM in terms of speed, its write operation is significantly slower than DRAM. In addition, PCM write operation consumes a greater amount of energy. According to [1], PCM main memory is 1.6 × slower and consumes 2.2 × more energy than a DRAM based main memory. Since PCM uses states of a chalcogenide alloy for storing information, toward changing state of the alloy, SET and RESET operation are done by exerting different current intensive pulses to it. This repetitive operations cause consecutive thermal expansion and contractions for phase change alloy, which result in contact detachment between heating element and the alloy [1]. This fact greatly limits number of possible reliable writes for PCM cells. PCM can only endure 10^8 to 10^9 reliable writes [10–12], while a DRAM memory can be written more than 10^{15} times [13].

To address the issue of limited number of writes in PCM, in previously proposed techniques it has been tried to reduce the number of write operations. Briefly, these works can be classified to five general categories. The first category uses a DRAM buffer or cache along with PCM main memory to help alleviate the number of writes [14,7]. The second category is wear levelling techniques which try to make writes as much uniform as possible [15]. The third category employs circuit level techniques to avoid redundant writes [16–18,1]. The forth category exploits information redundancy to tolerate failed cells [13,19,20]. Finally, the last category is based on coding methods to reduce bit flips [4,21–23].

In this paper we propose an *online data swapping* (ODS) scheme to prolong PCM lifetime. The main idea behind ODS is dividing each line of memory to chunks of data and then swap incoming write request between predefined sets of chunks to reduce the

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number of bit flips. In order to employ ODS in main memory, a circuitry is added between last level cache and main memory to perform the swapping process. Hence, ODS requires the addition of metadata information for each chunk of data. Due to aggressive updates in such metadata information, they are stored in DRAM memory. Experimental results carried out on PARSEC 3.0 [24] demonstrate that ODS improves the endurance of PCM based main memory endurance by about 48% and reduces its power consumption by approximately 46%. However, the average memory access time is increased by 1% due to the added circuitry.

The rest of this paper is organized as follows: Section 2 provides a brief background on Phase Change Memory and its read/write operations. Section 3 discusses previous work aiming at overcoming the issues of employing PCM in memory hierarchy. Section 4 details ODS. Section 5 presents experimental results. Finally section 6 concludes this paper.

2. Background

In this section we briefly explain the structure of a PCM cell. Then we more elaborate how read and write operations are performed in a PCM-based memory. Finally, we look at the limits which have hindered PCM from being used as a drop-in replacement for DRAM.

2.1. A brief overview of Phase Change Memory

A PCM cell is composed of a NMOS access transistor and a thin chalcogenide phase change alloy which is sandwiched between two electrodes. The phase change alloy is created from $Ge_2Sb_2Te_5$ alloy known as (GST). GST can have crystalline or amorphous states which represent logical value of one and zero. PCM read operation is performed by running a small current through the GST for a short time and measuring its resistance [25,26]. Write operation requires exerting an intense current for a long period of time to PCM cells to change its state.

PCM has various promising characteristics such as approximately zero leakage power, high density, non-volatility and immunity to radiation induced soft errors [2]. However, PCM write operation consumes a considerable amount of power and as PCM cells have a limited write endurance of 10^8 to 10^9 times, its wide deployment as a main memory technology has been hindered. Hence, reducing the number of writes in PCM can prolong its lifetime and reduce energy consumption.

3. Related work

Previous work on extending PCM lifetime can be classified into five categories. The proposed techniques in these categories are avoiding redundant writes, hybrid memory design, coding techniques, information Redundancy, and wear levelling. In the following we detail the related work in each category.

3.1. Avoiding redundant writes

Techniques in this category try to avoid writing the same values into cells by comparing the old value of data with the new value. Ref. [16] proposed data comparison write (DCW) scheme, a method that replaces a write operation with a read before write operation. The read operation takes place to check if incoming data and existing data are the same, creating a chance to avoid the write operation. Ref. [15] proposed changing PCM cell structure and adding a XNOR gate. This structure, reads existing contents of the bits and enables write operation only if the content of that bit must be flipped. This schemes requires changing the structure and design of PCM cells.

Ref. [17] has proposed a technique, the so-called Flip-N-Write (FNW) to reduce the number of unnecessary write operations. FNW firstly measures the hamming distance of incoming data and its inverse with the existing data. Then it decides whether the original data or its inverse should be written. FNW requires the addition of an extra flag bit which is used for retrieving the real data. As the best result for FNW is achieved when data have 2 bit length, and for each 2 bit data an extra flag bit is required, the overhead of FNW is much more than its effectiveness.

Ref. [27] has taken the advantage of removing useless write backs to increase PCM lifetime. Useless write backs are modified dirty blocks that are no longer used, for increasing lifetime these write backs can be avoided and eschewed from other write backs.

Their experimental results indicate that their method can have 26.2% lifetime enhancement.

3.2. Hybrid memory design

The aim in hybrid DRAM-PCM category is alleviating writes pressure in PCM part by sending frequent write intensive address or data to a small DRAM memory. These approaches can mitigate PCM endurance and energy consumption. Compared to PCM high write energy consumption, a small DRAM memory cannot affect overall energy consumption [28–32]. Ref. [31] is one of these methods which proposed a hybrid PCM-DRAM architecture that exploits CLOCK-DWF algorithm for predicting future writes, and sending these writes to DRAM part to improve PCM lifetime. Ref. [33] proposed a migration based cache replacement algorithm for hybrid DRAM-PCM memories to address low endurance and long latency of Phase Change Memory. Refs. [7,1,14] have proposed using write buffer based on DRAM technology to reduce write caused to PCM main memory and preventing wear-leveling failures. In their schemes when a page fault occurs, for avoiding PCM slow write operation it is first loaded to the DRAM write buffer and only if the page must be evicted from DRAM buffer it would be written back into PCM.

3.3. Coding methods

The aim of the methods in this category is to extend lifetime of non-volatile memories by reducing amount of received write traffic. In these methods, value locality of data words and exerting compression techniques to these high frequent redundant data sets is exploited in a way which decreases number of write caused to non-volatile memories.

Ref. [4] has observed that there is a large amount of zero extended values in memory access. They use this fact and propose a coding mechanism which stores these values in a compressed form. By taking advantage of multi level cell storage of PCM cells they store compact data values in single level cells and uncompressed data values in multi level cells.

Ref. [23] is motivated by an observation that there is a good amount of value locality in l2 cache transactions. They found 33 frequent data patterns and apply 1-LWC coding mechanism to these frequent data values for reducing number of writes operation caused to L2 STT-RAM based cache. Although this method can bring a good energy saving and write reduction, its usage is limited to embedded system that their data sets are known and do not change during system work as it needs static profiling.

3.4. Using information redundancy to tolerate failed cells

A failed cell in a PCM-based memory line due to a failure mechanism makes the whole line unusable. Therefore, using an