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Scanning Spreading Resistance Microscopy analysis of locally blocked implant sites

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ABSTRACT

We describe a well-controlled experiment enabling the generation of multiple locally blocked implant sites within an integrated circuit in order to evaluate Scanning Spreading Resistance Microscopy (SSRM) as analysis method. Transistor gate structures with polycrystalline (poly-)Si material and source/drain regions were locally affected by lower implantation dose due to the presence of Polystyrene Latex (PSL) spheres on the wafer surface which have the effect of blocking the implantation process. These sites are initially characterised using in-line defect density inspection, SEM voltage contrast, Atomic Force Probe (AFP) current imaging and $I(V)$ characterisation and then further analysed using Scanning Spreading Resistance Microscopy (SSRM). Subsequent analysis shows SSRM to be a very suitable and reproducible technique for visualisation of locally blocked implant sites in poly-Si gates. It is shown that the orientation of the prepared cross section is important for successful, artifact-free SSRM imaging. Our results demonstrate the potential of SSRM as a powerful analysis method for integrated device structures and set a reference system for topics like locally reduced poly-Si doping due to implant blocking or the presence of large poly-Si grains.

1. Introduction

Since conception in 1992 [1] and the first applications of the method in 1998 [2,3], SSRM has become an important analysis method for 2D imaging of semiconductor dopant profiles. It offers a high spatial resolution combined with a high dynamic range. These features make SSRM an appropriate technique for investigations into integrated device failure analysis caused by local deviations in dopant distributions. For example, device failure due to reduced dopant concentration in the poly-Si gate can result from local, unintended implant shadowing caused by residuals, particles or from the presence of very large poly-Si grains within the gate region. A well-understood model system is desired, that comprises the main feature of locally reduced poly-Si dopant concentration in order to investigate SSRM analysis capability and reproducibility as well as optimum sample preparation. Here, we report on a well-controlled experiment that fulfills these requirements. It was performed on a 130 nm CMOS product node. Although leading edge microprocessors and memory products for desktop and mobile application are manufactured using significantly smaller technology nodes, there are currently many products in fabrication and development that make use of technology ground rules well in the range of the 130 nm. For the later, analysis capability for device failure modes as described above is very significant.

SSRM is a secondary imaging mode derived from contact Atomic Force Microscopy (AFM) that maps two-dimensional resistance profiles with high spatial resolution [4]. As in other conductive AFM (c-AFM) techniques, in SSRM a conductive probe is scanned across the sample surface while a DC bias is applied between sample and probe. The resulting current flow is measured using a logarithmic current amplifier. The working principle of SSRM relies on the fact that the spreading resistance directly below the probe dominates the chain of serial resistance in the entire measurement path. Serial resistance contributions from the cantilever, probe, the contact and back contact must be significantly smaller. In this case the measured total

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resistance is to a first approximation equal to the spreading resistance $R(x,y)$:

$$R = \rho(x,y)/4\alpha,$$

where $\rho(x,y)$ = sample local resistivity, α = tip radius.

In the case of a semiconductor material, the local sample resistivity is related to the free charge carrier density, and therefore, to the local active dopant concentration.

Compared to other scanning probe microscopy techniques, very high forces between probe tip and sample surface are necessary to punch through the sample native silicon oxide and to achieve a phase transformation of the silicon right beneath the probe tip [5–10]. Boron doped full diamond probes with small tip radii are proven to be the best solution in order to achieve high lateral resolution and a high dynamic range of the electrical signal [11,12].

Despite the use of diamond as a probe tip material, tip wear is still a critical aspect for SSRM. Moreover, it is not only the probe tip that wears out, but also the sample surface is altered by indentation of the scanning probe tip. These effects limit the number of attainable images, especially for cross sections of integrated device circuits using small ground rules. In order to acquire significant measurement data as soon as possible during scanning and to prevent quick tip wear out, it is of great importance to choose the best position and orientation for the analysis site. In our case the area of interest is significantly increased and the sample topography is drastically reduced by avoiding metal plugs within the cross section. This prolongs tip life time and simultaneously reduces topography induced imaging artifacts in the electrical signal.

Another issue with SSRM can be the interpretation of results. Comparing two samples in order to check for differences requires the imaging conditions to be identical for both samples. This includes probe tip condition, contact force, gain values, imaging speeds and also sample preparation. Our experimental setup using locally blocked implant sites significantly reduces these effects, as the areas to be compared are next to each other on the same sample. Hence, changes in the imaging conditions can be avoided.

2. Experimental details

Core feature of our controlled experiment is the local selective blocking of specific implant layers during wafer processing, followed by complete characterisation of the resultant structure. Focus of this work is the analysis of locally blocked gate poly-Si implant. The analysis includes localisation of the artificially generated defect sites and electrical characterisation of affected structures. This information is then used as the basis for the evaluation of SSRM as a method for the investigation of dopant related variations within Complementary Metal Oxide Semiconductor (CMOS) technologies.

The local implant blocking was enabled by the application of Polystyrene Latex (PSL) spheres to the wafer front side. PSL spheres offer a well-defined spherical shape, and they are commercially available in calibrated sizes down to values smaller than 100 nm. PSL spheres are typically used for testing and calibration of inline wafer inspection tools [13]. The spheres are available in a bottled solution and application is done by simply spraying onto the wafer surface. For our experiment we have chosen spheres with a diameter of 4 μm. This size guarantees the complete blocking of the implant, even so the generated defects can still be considered as very local. A Scanning Electron Microscopy (SEM) image of a PSL sphere on top of our test wafer is shown in Fig. 1a.

A wafer lot was processed up to the point of the implantation step of interest. One wafer was then removed from the lot and exposed to the PSL spheres. The wafer was returned to the lot and the implantation of the source, drain and gate poly-Si was performed. Inline inspection using optical microscopy and SEM after the application of the PSL spheres before and after the implantation step has been carried out in order to distinguish between process base line defects and the artificially generated defects from our experiment. This inspection also provides the defect positions for the subsequent analysis. Post implantation, a cleaning step was performed in order to remove the PSL spheres. Next, the complete lot was processed according to the normal process flow, including self-aligned silicidation, deposition of an inter layer dielectric (ILD) and contact plug formation.

A Read Only Memory (ROM) field was chosen as a suitable region for analysis, since it provides both reference transistors and modified transistors adjacent to one another. The ROM design is a diffusion programmed type using an n-channel device in standard common ground NOR architecture. In order to rule out inaccuracies of the in line inspection coordinates, the defects were re-localised using SEM voltage contrast (Fig. 1b). To our advantage the blocked implant also affects source and drain regions, which do not form the typical low leakage diodes. These are observed as bright spots in the SEM voltage contrast image. The leaking diode behaviour was confirmed by conductive AFM scans combined with $I(V)$-characterisation of individual fail and reference contacts. For both, c-AFM measurements and the $I(V)$-characterisation, an Atomic Force Prober (Multiprobe) with tungsten probes was utilised [14,15]. The c-AFM current image as shown in Fig. 1c is obtained with sample substrate connected to the chuck at ground potential, and the scanning probe tip at 0.5 V. All reference contacts at S/D implant regions are expected to show only very small leakage currents (same colour value as the insulating oxide between the contacts). This is in contrast to the contacts in the area where the PSL sphere has blocked the implant, which exhibit significantly higher leakage currents. Both current image and $I(V)$-characteristic of the drain-substrate diodes (Fig. 1d) are in agreement with the SEM voltage contrast results and confirm the success of the local implant blocking.

3. II SSRM measurement

For SSRM preparation, the target site was marked and covered by a platinum protection layer using a Focused Ion Beam (FIB) technique. After mechanical grinding and polishing to the desired cross section position, the sample was loaded in the FIB system (FEI Helios system) for the final preparation step.

For SSRM measurements a Veeco Dimension 3100 was used, equipped with a Nanoscope IV controller and an SSRM application module for resistance measurement. Full diamond boron doped probe tips were used for image acquisition [16] with measurements carried out under ambient conditions. The samples were mechanically attached to the Veeco cross section sample holders. Electrical connection of the sample to the chuck was assured using conductive silver paint. The FIB deposited Pt protection layer electrically connects the source, drain and gate areas to the substrate by connecting the appropriate tungsten contacts. Adding the conductive silver paint on the silicon substrate and the sample holder is sufficient to guarantee the conduction of the measurement current from the surface of the cross section to the back contact.

The FIB prepared area of interest can be easily found using the optical microscope of the AFM. In order to conserve tip life time and also the sample for maximum number of SSRM images, after the initial approach to the cross section surface full scans were inhibited for finding the correct imaging position. The contact level edge of the sample was located by scanning 2 μm lines perpendicular to the edge and adjusting the spatial offset accordingly. Once the sample edge is detected, the target position along the gate poly line can be found by scanning parallel to the sample edge below the active area top edge. Due to the curtaining effect induced by