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TiN/titanium–aluminum oxynitride/Si as new gate structure for 3D MOS technology

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ABSTRACT

Titanium–aluminum oxynitride (TAON) has been used as high-*k* gate dielectric for planar MOS devices (capacitors and transistors) and obtained by Ti/Al e-beam evaporation, with additional electron cyclotron resonance (ECR) plasma oxynitridation on Si substrates. Thus, planar MOS (Al/TAON/Si) capacitors were characterized by TEM and EDS analyses, and the film formation with thickness of 6.7 nm and with Ti, Al, O and N into the TAON dielectric bulk is confirmed. However, for future 3D device technology application, these films have been not investigated. So, 3D MOS capacitors with Al/TAON/Si (as control sample) and TiN/TAON/Si gate structures for 3D technology were fabricated. Al/TAON and TiN/TAON layers on 3D gate region must present conformal coverage, which is a mandatory requirement for 3D transistors, such as FinFET. To characterize the TAON conformal coverage for this technology, the gate structure formed by Al/TAON/Si for FinFETs were fabricated and the "Fin" structures were obtained using a Focused Ion Beam (FIB) system to become thinner the width of active area to get the "Fin" structure. *C–V* curves of these structures were performed at 1 MHz, and the three *C–V* curve regions (accumulation, depletion and inversion) are well defined for all capacitors, indicating that the conformal coverage on the 3D and FinFET gate regions can be occurred. Furthermore, these results indicated that TiN/TAON layers can be used as a new alternative for 3D MOS structures.

1. Introduction

High-*k* insulators for the next generation (sub-32 nm CMOS (complementary metal–oxide–semiconductor) technology), such as titanium–aluminum oxynitride (TAON), have received considerable attention due their electrical and physical properties, which come from the composition of titanium oxide and aluminum oxide, such as higher dielectric constant ($k \sim 80$) and higher band gap (e.g. ~8.8 eV), respectively. Furthermore, this composition can reduce the undesirable effects on sub-32 nm MOS devices with gate dielectrics of titanium oxide or aluminum oxide, consequent high leakage current due to the band offset of 2.8 eV of Al_2O_3 [1], and EOT higher than 2 nm due to relatively low *k* between 8 and 10, respectively [1,2,8]. In this work, titanium–aluminum oxynitride (TAON) gate insulators were obtained by Ti/Al e-beam evaporation, with additional electron cyclotron resonance (ECR) plasma oxynitridation on Si substrates, respectively. ECR system is downstream plasma reactor, where a separate control of ion energy and ion flux is possible. The reactor can operate at low pressures (1–50 mTorr) allowing a drastic reduction of the ion surface sputtering. A 2.45 GHz microwave source generates the plasma at high power (up to 1000 W) a 13.56 MHz RF power source biases separately the sample chuck. The 2.45 GHz ECR source and RF chuck power control the ion flux and ion energy, respectively, allowing low temperature, low pressure and low damage chemical vapor deposition (CVD) or plasma Si surface oxidation and/or nitridation [3]. A 300 nm Al thick layer was deposited by DC sputtering process on TAON dielectric. Thus, in Ref. [4], planar MOS capacitors with Al/TAON/Si structure were fabricated, with a TAON film named TAON-1. In this work, these planar MOS capacitors were characterized by TEM and EDS measurements to extract the direct physical TAON film thickness, and the composition, which can indicate the presence of Ti, Al, O and N in the TAON film, respectively. With the EOT of 1.5 nm (extracted from *C–V* curves presented in Ref. [4]) and TAON physical thickness value from TEM analysis, the dielectric constant can be estimated. Also, in Ref. [4], planar nMOSFETs with Al gate electrode and TAON gate dielectric (named TAON-2) were fabricated and characterized by current–voltage (*I–V*) curves. From these nMOSFETs electrical characteristics, parameters such as subthreshold slope of 80 mV/decade and EOT of 0.87 nm were determined. The results have indicated that the obtained TAON-2 film is a suitable gate insulator for the next generation MOS devices [4]. Thus, in this work, the TAON-2 film is investigated as a new alternative to replace the current HfO_x films for FinFET devices, which are transistors with 3D MOS gate structures. In this context, 3D MOS capacitors with Al/TAON/Si (as control sample) and TiN/TAON/Si gate structures for FinFET technology were fabricated.

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Al/TAON and TiN/TAON layers on 3D region must present conformal coverage, which is a mandatory requirement for 3D transistors, such as FinFET. The 3D structures were obtained by sequential lithography and SF_6/Ar plasma etching. The TAON was formed on Si substrates with these structures. To finalize the 3D MOS capacitor, Al (300 nm) and TiN (300 nm) gate electrodes were deposited (by sputtering) and patterned (by lithography process) on TAON/Si structures in two different samples. *C–V* measurements of these structures were performed at 1 MHz. The results can indicate if the TiN/TAON structure is (or not) a new alternative for 3D device technology to substitute the TiN/HfO_x structures, which have been used for this application [2,9]. Furthermore, on Si substrates, 3D Al/TAON gate structures for FinFETs were fabricated. Al/TAON layers on "Fin" region must present conformal coverage, which is a mandatory requirement for 3D transistors, such as FinFET. The "Fin" structures were obtained by sequential photo-lithography and SF_6/Ar plasma etching to define the active area. Focused Ion Beam (FIB), which is a dual-beam (gallium ion and electron) system, was used to decrease the width (using the gallium ion beam with energy of 30 keV and current of 2 nA) the width of active area to get the "Fin" structure with width (Wfin) of 100 nm. It is important to notice that the directional gallium ion beam used in this process can adjust the roughness of the Fin vertical walls. This occurs because this ion etching is completely directional anisotropic process, without lateral etching, which can reduce the wall roughness. The following step is the TAON formation on Si substrates. After, to get the FinFET gate structure (3D MOS capacitor), Al (300 nm) gate electrodes were deposited (by sputtering) and patterned (by lithography process) on TAON/Si structures. *C–V* measurements of these structures were performed at 1 MHz. The results, such as effective charge density in MOS structure and no distortion in *C–V* curves, can indicate that the TAON films are conformal on Fin structure and can be used as a new alternative gate dielectric for FinFET device technology, because, nowadays, the gate dielectric is HfO_x film [2,7,9].

2. Experimental

2.1. 3D MOS capacitor fabrication

3D MOS capacitors were fabricated on p-type single-crystal Si (100) wafers with resistivity ranging from 1 to 10 Ω cm. The substrates were cleaned by RCA method, such as used in Refs. [5,10] for application in Gate-All-Around Si Nanowire MOSFETs with high-*k*/metal-gate, which are 3D transistors. The 3D structures on Si wafers (mesa shape) were obtained by sequential lithography and SF_6/Ar plasma etching of a 200 nm thick Si layer, using a gas mixture with SF_6:Ar flow ratio of 12:35 sccm, pressure of 50 mTorr and power of 500 W, resulting in silicon etch rate of 0.1 μm/min. An organic cleaning was carried out to remove the resist. To finish the wafer cleaning process, RCA method [10] was used. The used TAON-2 dielectric gate was obtained, with the same conditions for planar MOSFETs in Ref. [4], as follow: 0.75 nm titanium (Ti) and 0.25 nm aluminum (Al) sequentially deposited on Si substrates by vacuum e-beam evaporation of 99.9999% of Ti and Al metals, respectively, without any substrate heating. The evaporation pressure was 3.10^{-8} Torr, and Ti and Al evaporation rates were of 0.1 nm s^{-1}. The ECR plasma oxynitridation process was carried out at O_2:N_2:Ar flow ratio of 3:10:20 sccm. In Ref. [4] is presented the motivation, which is the formation of high-k dielectric with EOT thinner than 1 nm, to change the Ti/Al stacked layer thickness values. So, on one part of wafers, 300 nm thick aluminum layer was deposited by DC sputtering process to form the 3D MOS capacitor structure gate contacts. These samples were named control 3D capacitors. The sputtering condition for Al electrodes deposition were Ar flow of 60 sccm (pure argon ambient) and DC power of 1000 W. A second part of wafers, aluminum gate electrodes were changed by titanium nitride (TiN) electrodes. TiN film has been obtained by DC reactive sputtering deposition of a Ti (99.95% purity) target, in an N_2/Ar ambient (with flow ratio of 10/80 sccm, respectively), using a DC power of 1000 W. Using a four-probe technique, electrical resistivity of TiN film of 270 μΩ cm was obtained [6]. The both kind of electrodes were patterned with a mask composed of frame shape with area of 9360 μm^2 (see Fig. 1). About 300 nm aluminum backside substrate contacts were deposited by DC magnetron sputtering using argon flow of 60 sccm and power of 1000 W, in pure argon ambient. Then, these devices were sintered in a conventional furnace in forming gas at 450 °C for 20 min.

2.2. 3D MOS gate fabrication for FinFET

3D Al/TAON-2 gate structures for FinFETs were fabricated using same Si wafers, RCA cleaning process [10], lithography and SF_6/Ar plasma etching to define active area presented in previous item about 3D MOS capacitor fabrication. After the formation of the 3D structures (active area region of FinFET (Fig. 2)), Focused Ion Beam (FIB), which is a dual-beam (gallium ion and electron) system, was used to become thinner (using the gallium ion beam with energy of 30 keV with 3 nA) the width of active area to get the "Fin" structure with width (Wfin) of 100 nm. Fig. 3 presents all steps of Fin thinning process. The next step was the TAON formation on Si substrates. The TAON-2 formation was carried out with the same conditions, which were used to get the gate dielectric for planar n-MOSFET [4] and for 3D MOS capacitor previously presented. After, 300 nm thick aluminum layer was deposited by DC sputtering process to form the 3D MOS capacitor structure gate contacts with the same conditions presented in previous item about 3D MOS capacitor fabrication. The Al electrodes were patterned with a mask composed of frame shape with area of 9360 μm^2 (Fig. 2). So, 300 nm aluminum backside substrate contacts were deposited by DC magnetron sputtering using argon flow of 60 sccm and power of 1000 W, in a pure argon ambient. Then, these devices were sintered in a conventional furnace in forming gas at 450 °C for 20 min. Al/TAON layers on "Fin" region must present conformal coverage, which is a mandatory requirement for FinFET.

2.3. Capacitance–voltage (C–V) measurements

All capacitors (3D MOS and FinFET gate structures) were used to obtain capacitance–voltage (*C–V*) measurements to investigate that if, in *C–V* curves, the accumulation, depletion and inversion regions are presented. Thus, it can indicate that the Metal/TAON conformal coverage on 3D gate structures occurs, that is a mandatory requirement for 3D device technology.

3. Results and discussion

3.1. Planar MOS capacitor – TEM and EDS analyses

In Ref. [4], the direct physical film thickness measurements extracted by transmission electron microscopy (TEM) analysis of Al/TAON-1/Si structures was not presented. So, in this work, TEM and Energy Dispersive X-ray (EDS) analyses were carried out in planar Al/TAON-1/Si capacitors, and are presented in Fig. 3. TAON-1 layer was formed on p-type Si (100) wafers [4], using 0.5 nm Titanium (Ti) and 0.5 nm aluminum (Al) films were sequentially deposited by vacuum e-beam evaporation of 99.9999% of Ti and Al metals, respectively, without any substrate heating. The evaporation pressure was 3.10^{-8} Torr, and the Ti and Al evaporation rates were of