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Design and implementation of multi-mode routers for large-scale inter-core networks

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ABSTRACT

Constructing on-chip or inter-silicon (inter-die/inter-chip) networks to connect multiple processors extends the system capability and scalability. It is a key issue to implement a flexible router that can fit into various application scenarios. This paper proposes a multi-mode adaptable router that can support both circuit and wormhole switching with supplying flexible working strategies for specific traffic patterns in diverse applications. The limitation of mono-mode switched routers is shown at first, followed by algorithm exploration in the proposed router for choosing the proper working strategy in a specific network. We then present the performance improvement when applying the mixed circuit/wormhole switching mode to different applications, and analyze the image decoding as a case study. The multi-mode router has been implemented with different configurations in a 65 nm CMOS technology. The one with 8-bit flit width is demonstrated together with a multi-core processor to show the feasibility. Working at 350 MHz, the average power consumption of the whole system is 22 mW.

1. Introduction

Hosting many cores in a single chip, e.g. multiprocessor system-on-chip (MPSoC) [1,2], is a prevailing solution to keep increasing single chip performance. Tens or hundreds of cores have been connected by the network on chip (NoC) to supply very high performance [3,4]. Integrating even more cores is foreseeable in the billion-transistor era [5]. The inevitable complex traffic patterns generated among those cores necessitate the design of a flexible router that can fit into various scenarios.

On the other hand, the ability to extend the network for integrating more cores is one of the advantages using NoCs. The design is usually determined by the highest performance required for the worst case application, and the scalability is constrained once the chip is physically implemented. As a result, designers put much effort into increasing core capability and network capacity to achieve extremely high peak performance. Meanwhile, physical design, verification, testing, heat dissipation, yield, etc. are becoming the problems when scaling up the chip size [6–8]. Nevertheless, for most of applications, not all the cores are necessary leading to low energy and area efficiency. Instead, a processor cluster can provide more scalability capable of grouping the suitable number of processors and tailoring the network on demand. The drawback is the slow interconnection speed, high power consumption and low energy efficiency.

By stacking the silicons vertically in 3D NoC [9,10] or constructing the network in package (NiP) [11] for inter-silicon (inter-die/inter-chip) network, scalability is extended compared with MPSoCs. The purpose is to provide on-demand performance for the specific application. In this case, high energy and area efficiency with low implementation cost are achievable. Furthermore, the problems resulted from scaling up the single silicon are also solvable.

For both the large-scale on-chip and the inter-silicon network, i.e. inter-core network, network sizes and task mapping algorithms are varied with different applications. A flexible router with adaptability to diverse application scenarios is highly demanded. The state-of-the-art routers mainly focus on increasing network utilization and throughput other than adapting to different traffic patterns. Even circuit and wormhole switching are combined in some literatures [12,13], whereas they are not free to be switched for transmissions in diverse traffic patterns.

In this paper, we merge circuit switching (CS) with wormhole switching (WS) in one router to realize a multi-mode traffic-adaptive router. Two switching techniques share physical channels and control logics, and the transmissions by circuit switching are given higher priority to use the resources. A proper working mode will be selected based on the analysis of traffic patterns. To show

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the advantages of using multi-mode over mono-mode switching, we also implement parameterized routers for both circuit and wormhole switching, respectively. All the routers are implemented in synthesizable hardware at register-transfer level (RTL) for cycle-accurate simulation and precise cost evaluation. We further use them to construct scalable networks with different sizes to explore the algorithm of selecting the suitable switching mode for a specific application. A demonstration of the proposed multi-mode router together with a multi-core processor is fabricated in 65 nm low leakage CMOS technology to show the feasibility.

The main contributions of this paper include the following:

- A flexible and scalable router architecture supporting multi-mode switching adaptively is proposed and implemented;
- Quantitative study of various factors on choosing the suitable switching mode is performed;
- One node integrating the router together with a multi-core processor is fabricated in 65 nm CMOS technology, and ready for constructing the network.

The remainder of this paper is organized as follows. Related work is discussed in Section 2. Section 3 details the proposed router architecture with the multi-mode adaptable switching scheme. The simulation platform together with evaluation metrics is described in Section 4. Section 5 shows the performance comparisons. Implementation results are given in Section 6. Finally, we draw conclusions in Section 7.

2. Related work

Design of routers for inter-silicon networks has been studied in many literatures. In [14], the authors utilize inductive-coupling links to transmit the data between different planes in 3D NoC. Rings are constructed to connect those routers, while packet switching is only supported with the bubble flow control algorithm. Reference [15] uses 3D-mesh topology to connect various processing elements, and packet switching together with credit-based flow control is employed for data transmission. Most of the studies for 3D NoC focus on the selection of suitable topology and routing algorithm to decrease the use of vertical links and increase the efficiency, while a flexible router with the capability of choosing the suitable switching mode according to a specific application scenario is also necessary. Besides stacking the silicons vertically, placing them in one plane to build the NiP is also a solution to construct the inter-silicon network [11]. Nevertheless, a scalable router is still missing.

The concept of combining circuit switching with packet switching to supply throughput-guaranteed service while incre asing the network utilization for on-chip networks has also been discussed. The SDM (Space-Division Multiplexing) is used to combine circuit switching and packet-switching in one router in [16,17]. However, the resources for two switching schemes are physically separated, resulting in larger area overhead and power consumption. A mixed circuit/– packet switched network is also implemented in [13]. The packet-switched network is only used to establish the dedicated link for circuit-switched network, but not for data transmission.

In [18], virtual point-to-point (VIP) dedicated links are added to a packet-switched network to improve performance and reduce the power consumption. Two schemes are used for link establishment: static VIPs for traffic patterns known in advance, and dynamic VIPs for traffic patterns unknown. In static VIPs, data transmissions will be firstly tried with VIP links, and the failed ones will be processed by packet switching. In dynamic VIPs, a centric root node is required to configure the whole network, and the traffic information needs to be collected. In our proposed router architecture, the selection of a specific switching scheme is based on the property of transmissions, and dedicated links are established dynamically and distributively, thus enabling good scalability.

Guaranteed services (GS) and best-effort services (BE) are both delivered in [19]. BE flits can use channels only when the GS does not use them. GS transmissions will share physical channels in a TDM (Time-Division Multiplexing) fashion and use BE packets to setup and tear down the dedicated connections. Source routing is employed for BE packets. In our scheme, circuit-switched messages will not share channels with each other to keep the maximum bandwidth for each transmission, and dynamic routing is employed for wormhole-switched messages to make the network flexible and scalable.

The authors in [20] propose a hybrid circuit switching (HCS) scheme. Circuit switching is implemented together with wormhole switching in one router and shares the same physical channels. A setup request will be sent out to search for unused circuits, and if there is any available circuit, circuit switching will be used for transmission. Otherwise, packet switching will take over. Meanwhile, if a packet-switched flit is using the router, the circuit-switched flit will be latched and wait until the router is released. In contrast to their scheme, the decision of using either circuit switching or wormhole switching is made by the initial node in our proposed network by evaluating the performance of the whole system and will not be changed during the transmission. We give the highest priority to circuit switching to ensure low latency. Circuit-switched messages can also preempt the links being used by wormhole-switched messages. Wormhole-switched messages can still utilize the related physical channels in the setup phase for circuit switching. This can alleviate traffic congestion and increase link utilization.

The hybrid scheme is also studied in [21] to combine circuit switching and packet switching. The path allocation algorithm is proposed. However, path allocation is performed statically with all network information collected in the host processor. It will become the obstacle for the router adapting to different application scenarios.

Compared with other hybrid switching schemes, our proposed multi-mode router is able to provide circuit switching (CS) only, wormhole switching (WS) only and mixed CS/WS modes for diverse application scenarios adaptively. Our focus is to demonstrate the advantages of dynamically selecting the switching mode when network sizes, traffic patterns and scenarios are variable for inter-core networks.

3. Architecture

In the following sections, we use *messages* to represent the data transmitted from source to destination by circuit switching or wormhole switching. Furthermore, *circuit-switched messages* are the messages that need to be sent in circuit switching mode, while *wormhole-switched messages* are the ones used in wormhole switching mode. After this clarification, the proposed router architecture together with the corresponding switching scheme is presented in the following section.

3.1. Router structure

The proposed multi-mode adaptable router structure supporting both circuit switching (CS) and wormhole switching (WS) is shown in Fig. 1, which is designed for mesh-based NoCs. There exist five pairs of input and output ports to connect four neighboring routers directly and one local device through a network