Journal of Electron Spectroscopy and Related Phenomena 203 (2015) 1–7

Contents lists available at ScienceDirect

Journal of Electron Spectroscopy and Related Phenomena

journal homepage: www.elsevier.com/locate/elspec

Backside versus frontside advanced chemical analysis of high-k/metal gate stacks

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ARTICLE INFO

Article history:
Received 18 December 2014
Received in revised form 3 April 2015
Accepted 29 April 2015
Available online 11 May 2015

Keywords:
Metal/high-*k* stack
HfO_2
Backside analysis
XPS
Auger depth profiling
ToF-SIMS

ABSTRACT

Downscaling of transistors beyond the 14 nm technological node requires the implementation of new architectures and materials. Advanced characterization methods are needed to gain information about the chemical composition of buried layers and interfaces. An effective approach based on backside analysis is presented here. X-ray photoelectron spectroscopy, Auger depth profiling and time-of-flight secondary ions mass spectrometry are combined to investigate inter-diffusion phenomena. To highlight improvements related to the backside method, backside and frontside analyses are compared. Critical information regarding nitrogen, oxygen and aluminium redistribution inside the gate stacks is obtained only in the backside configuration.

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1. Introduction

Downscaling of complementary metal oxide semiconductor (CMOS) transistors beyond the 14 nm technological node requires the implementation of new planar or 3D architectures [1]. The control of the materials properties and interfaces during integration is one of the main issues to ensure good device performances. In particular, electrical properties might be affected by inter-diffusion phenomena occurring during post-deposition steps, such as high-temperature annealing used for source (S) and drain (D) formation in the gate first approach. These phenomena still exist at a lower level in the gate last integration scheme, which is a promising solution considered today to better control the transistor composition because of its low thermal budget [2].

The gate stack designed for the sub-14 nm devices of the gate last technology is made of ultrathin layers such as the SiO_2 Inter-Layer (IL), the high permittivity HfO_2 oxide and the TiN-based work function metal gate [3,4]. An additional low resistance contact metal gate covers these layers that are deposited on a silicon substrate. In the particular case of simple MOS capacitors, realized here for gate effective work function (EWF) and equivalent oxide thickness (EOT) evaluation, a thick contact metal of about 150 nm is deposited. Therefore, the chemical analysis of the buried layers in the stack, i.e. the SiO_2, HfO_2 and TiN-based layers and their interfaces, becomes a real challenge when performing a frontside analysis, i.e. from the metal gate side. There is a real need for a method allowing a relevant analytical investigation.

Removal of the upper thick metallic layers by chemical etching is an option [5]. However, the chemical etch selectivity is not always sufficient to preserve the underlying thin metallic and oxide layers. Deposition of a metal gate, which is thinner than the real integrated one, is not appropriate because the stack is no more representative of the final device. The overall thermal budget is not the same and thus the final structure and chemical composition might be modified. Alternatives are based on ion sputtering and sequential chemical analysis but these methods are known to suffer from potential artefacts such as preferential sputtering [6]. Moreover, ion sputtering may generate roughness, in particular when crossing the thick metal gate. The depth resolution quickly degrades, thus preventing a precise analysis of the elements depth distributions in the region of interest.

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http://dx.doi.org/10.1016/j.elspec.2015.04.022
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One efficient way to get the chemical composition of these buried layers consists in working on cross-sections with transmission electron microscopy based techniques such as energy dispersive X-ray spectrometry (STEM-EDX). This option, which needs specially prepared thin samples transparent to electrons, will be considered in another paper. In this work, we have implemented another approach, namely the backside analysis. The basic idea is to remove the Si substrate and perform surface or in-depth chemical analyses directly on the region of interest. Compared to transmission electron microscopy, which brings localized information, this method provides complementary bulk information at a larger scale. This approach was proved to be efficient for depth profiling of Hf containing materials, as reported in the literature [7,8]. Indeed, hafnium implantation upon sputtering is reduced when analysing the stack from the backside.

In this paper, we have implemented backside sample preparation of gate stacks designed for the gate last flow. Then, Auger electron spectroscopy (AES), time of flight secondary ions mass spectrometry (ToF-SIMS) and X-ray photoelectron spectroscopy (XPS) are combined to investigate elemental depth distributions as well as chemical bonding states within the area of interest located near the silicon substrate. Comparisons between backside and more conventional frontside analyses are performed to highlight the benefits of the backside approach.

2. Experimental details

2.1. Sample fabrication and backside preparation

HfO_2/TiN/TiAl/TiN/W and HfO_2/TiAlN/TiN/W stacks are considered for this demonstration. The 2 nm-thick HfO_2 layer is deposited using atomic layer deposition (ALD) at 360 °C on blanket 300 mm Si(1 0 0) wafers covered by a 0.7 nm-thick thermal SiO_2-IL bottom oxide. This is followed by a short post deposition annealing at 650 °C. The work function metal gate is made of two successive thin layers, a TiN (2 nm) layer followed by a TiAl (2.5 nm) layer, or a single 3.5 nm-thick TiAlN layer. In both cases, a 10 nm-thick TiN layer is deposited on top of the stack. These metal films are deposited using physical vapour deposition (PVD). The contact metal gate is finally obtained by depositing a 5 nm-thick TiN layer using metal organic chemical vapour deposition (MOCVD) at 395 °C followed by a 150 nm-thick W layer deposited by chemical vapour deposition (CVD) at 370 °C. For frontside XPS analyses, specific samples with a thinner gate are prepared. A single 2 nm-thick TiN layer replaces the TiN(10 nm)/TiN(5 nm)/W(150 nm) tri-layer.

Backside sample preparation is performed following a protocol previously described in [7]. The sample is first mounted up-side down on a patterned substrate. Then, a mechanical thinning of the Si substrate is performed until reaching a few μm. Finally, chemical etching of the remaining silicon is performed using tetramethylammonium hydroxide (TMAH). A flat and smooth surface is obtained, the surface roughness being measured below 0.3 nm by atomic force microscopy (AFM) (Fig. 1). The SiO_2 interfacial layer is preserved thanks to the high selectivity of TMAH for Si, the etching rate being four order of magnitude higher for Si than for SiO_2 [9].

In this work, this protocol is optimized for the complex stacks designed for the gate last flow, including the full metal gate. This means that the remaining part of the Si substrate has to be thicker (4–5 μm), before the chemical etching process, to prevent further delamination of the underlying layers through this etch process, due to high residual stress. The stacks and preparation methods used for both backside and frontside approaches are summarized in Fig. 2.

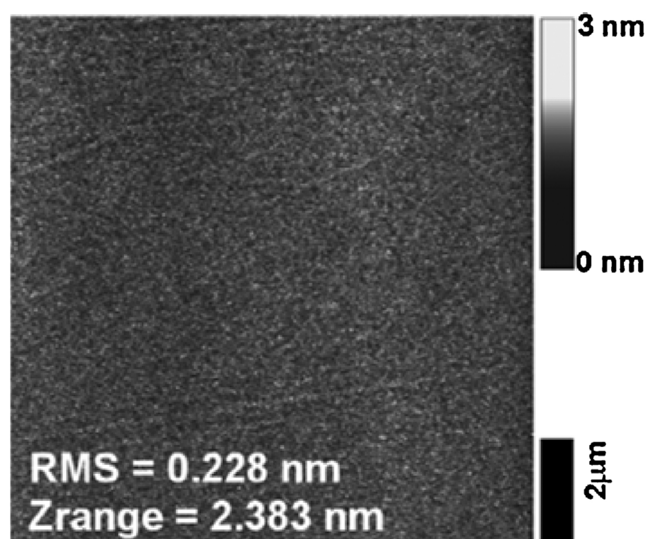

Fig. 1. AFM image of the sample obtained after backside preparation.

2.2. X-ray photoelectron spectroscopy (XPS)

Backside XPS analyses are carried out with a spectrometer from Oxford Instruments, equipped with a monochromated Al*K*α source ($h\nu$ = 1486.6 eV). Photoelectrons are detected at a take-off angle of 90° with respect to the sample surface. The pass energy is set at 20 eV leading to an overall energy resolution of 650 meV.

Frontside XPS measurements are performed on a ThermoFisher Scientific Theta 300 spectrometer, equipped with a high resolution monochromatic Al*K*α X-ray source. The overall energy resolution is 700 meV. The core level spectra are accumulated over the 20–80° emission angle range.

In the normal collection, for both backside and frontside configurations, the sampling depth is estimated to be 5 nm taking an inelastic mean free path of 1.7 nm for N1s photoelectrons in HfO_2 [10]. The size of the probed area is around 1 mm^2 for both configurations.

2.3. Auger electron spectroscopy (AES)

AES is performed with a PHI 700Xi scanning Auger nanoprobe equipped with a cylindrical mirror analyser ($\Delta E/E$ = 0.5%) and a co-axial electron gun, normal to the sample. The electron beam energy and current are fixed to 10 keV and 10 nA. The analysed area is 100 μm^2. Depth profiling is performed at grazing incidence (28°) with argon ions accelerated at 500 eV (~500 nA current).

2.4. Time-of-flight secondary ions mass spectrometry (ToF-SIMS)

ToF-SIMS is carried out using a dual beam ION-TOF V system. Depth profiles are acquired using a Cs^+ sputter gun at low energy (500 eV, 16 nA) and negative ion detection mode with a Bi_3^+ primary ion beam at high energy (25 keV) and low current (0.25 pA), for both frontside and backside approaches. The sputter beam is operated at low energy and the primary ion beam at very low current to minimize sputter-induced artefacts and preserve the depth resolution. The analysed area is 300 × 300 μm^2. The depth profiles are obtained by measuring the CN^-, TiN^-, AlN^-, C^-, O^- and HfO_2^- ions. The choice of the cluster ions as detected species, except for C^- and O^-, is done to maximize the sensitivity, in order to compensate for the small Bi_3^+ beam current.

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