Microelectronic Engineering 121 (2014) 156–161

Contents lists available at ScienceDirect

Microelectronic Engineering

journal homepage: www.elsevier.com/locate/mee

Oxidation smoothening of silicon machined micro- and nano-scale structures

S. Azimi [a,b,*], Z.Y. Dang [a], M.B.H. Breese [a,b]

[a] Centre for Ion Beam Applications (CIBA), Department of Physics, National University of Singapore, Singapore 117542, Singapore
[b] Singapore Synchrotron Light Source (SSLS), National University of Singapore, 5 Research Link, Singapore 117603, Singapore

ARTICLE INFO

Article history:
Received 11 November 2013
Received in revised form 2 April 2014
Accepted 24 April 2014
Available online 10 May 2014

Keywords:
Silicon micromachining
Surface roughness
Ion beam irradiation
Electrochemical anodization
Two- and three-dimensional structures
Free-standing

ABSTRACT

We have developed a process to machine bulk silicon in two- and three-dimensions shapes and structures. Here we briefly introduce this process and give examples of the types of surface profiles and three-dimensional geometries which can be fabricated. One of the limitations, as with all forms of silicon machining is the final surface roughness, as this introduces losses, for example in light propagation through photonic devices. Here we describe various contributing factors to the surface roughness and options to reducing it. Under optimized conditions roughness values of less than 1 nm can be achieved.

1. Introduction

Recent developments in micro- and nano-fabrication technologies have opened up opportunities in diverse fields and contributed to a new phase for developments of miniaturized devices. Although a variety of different materials can be used, silicon is the material of choice because of the availability of wide range of manufacturing facilities, mostly developed for integrated circuit fabrication. It is also a semiconductor with unique mechanical and optical properties [1]. A technique capable of fabricating complex geometries of silicon structures and shapes can contribute significantly to the development of the new generation of micro- and nano-devices.

We recently developed a process for micro- and nano-machining of a variety of structures and components in silicon using a combination of ion irradiation and electrochemical anodization. Different types of silicon surface patterns, three-dimensional wires, complex free-standing structures, etc., were fabricated [2,3]. For many applications, controlling and/or reducing the surface roughness [4–6] is a key factor, such as holographic silicon surfaces [7], low loss silicon photonic components [8], micro/nanoelectromechanical systems [9–11], high q-factor nanoresonators [10,12] and microcavities [13,14]. For commercially available silicon wafers, the surface roughness is usually less than 0.2 nm. Any fabrication process is therefore likely to degrade this extremely smooth surface.

The specular reflection, R_s, of a wavelength λ, from the root mean square surface of roughness σ of a perfect conductor at normal incidence is:

$$R_s = R_o \exp[-(4\pi\sigma)^2/\lambda^2] \quad (1)$$

where R_o is the reflection from a perfectly smooth surface of the same material [15]; clearly a low roughness is desirable to achieve a high reflectivity. For infrared light scattered by the surface roughness of silicon waveguides, a number of studies have been conducted [8,16,17]. In [16] it was found that the measured propagation loss through a waveguide fabricated with a typical sidewall roughness of 9 nm reduced to a minimum value of 0.1 dB/cm when the roughness was reduced by oxidation to 0.5 nm. In another example [8] oxidation reduced the propagation loss through waveguides fabricated using our process from 3 dB/cm to ~1 dB/cm, with the surface roughness being reduced from ~17 nm to 3 nm. One puzzling aspect of our prior work was the large surface roughness values measured directly after fabrication and how rapidly these were reduced by the effects of thermal oxidation. Therefore, it is important to better study surface roughness of silicon components fabricated using our machining technique and find means of minimizing this, to enhance its potential for fabricating different

* Corresponding author at: Centre for Ion Beam Applications (CIBA), Department of Physics, National University of Singapore, Singapore 117542, Singapore. Tel.: +65 65164135.
E-mail address: sara@nus.edu.sg (S. Azimi).

http://dx.doi.org/10.1016/j.mee.2014.04.033
0167-9317/

arbitrary-shaped smooth silicon micro- and nano-structures [2,18]. Here we describe examples which highlight the dual effect of oxidation in not only reducing the roughness of the silicon surface, but also, and just as importantly, remove all residual traces of low porosity silicon from the anodized surfaces.

Our machining process uses high-energy ion irradiation, typically 100–2 MeV protons and helium ions, of p-type silicon wafers, followed by electrochemical anodization in a hydrofluoric acid (HF) solution. Anodization of silicon forms porous silicon (PSi) where the surface is partially dissolved away, leaving a sponge-like network in which nanocrystalline silicon islands remain [19,20]. Ion irradiation of silicon causes crystalline damage (Fig. 1(a)), mainly as vacancy-interstitial pairs. These act as trap levels where charge carriers undergo recombination, reducing the hole density and increasing the resistivity along the ion trajectories [21]. Ion irradiation thus alters the hole current flow during subsequent electrochemical anodization, allowing the anodization rate to be slowed/stopped for low/high fluences. For moderate fluences the anodization rate is selectively stopped only at depths corresponding to the high defect density at the end-of-range, giving a machining technique for true 3D silicon micro/nano-fabrication. The underlying silicon structures which are buried in a PSi layer may be easily revealed by removing the PSi with dilute potassium hydroxide (KOH). This 3D silicon micro and nanomachining process has the potential to provide a wealth of new types of structure for silicon photonics, M/NEMS and BioMEMS.

2. Precisely controlled 3D silicon and PSi surface patterning

This machining approach can be used for fabricating precisely-controlled 3D silicon and PSi surface patterns. At a low fluence irradiated line, PSi is formed at the surface, and only close to the ion end-of-range does the defect density become high enough to allow the formation of a narrow tip at the top of the end-of-range core, Fig. 1(b). So if the anodization is stopped just when the tip of the core is exposed, a sharp region forms, Fig. 1(c). In comparison, in wider, heavily-irradiated regions, anodization is totally stopped, while PSi forms on either side, producing a tall, wide silicon region. Fig. 1(c) shows the resultant shapes of the low-fluence, narrow

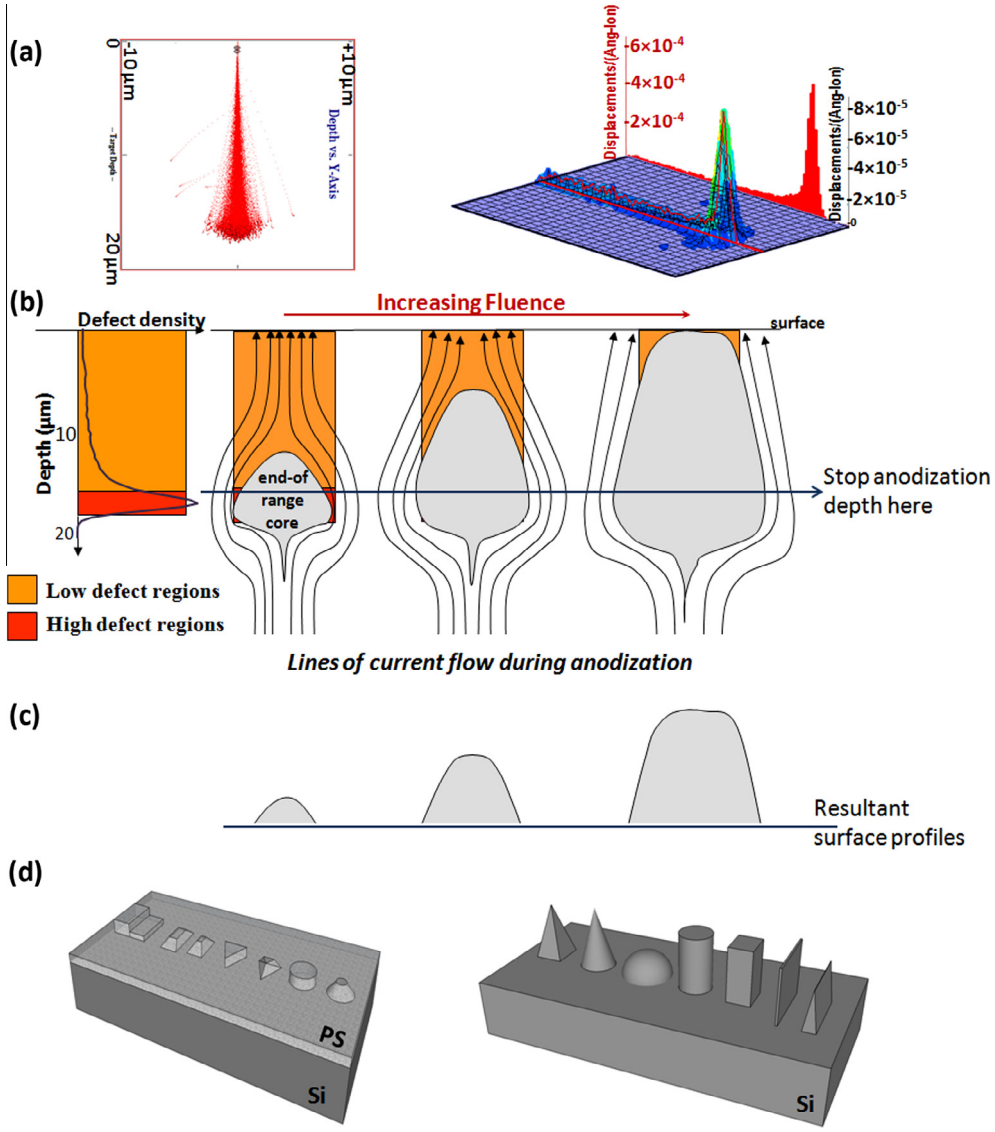

Fig. 1. (a) SRIM simulated trajectory and defect density plot versus depth for 1 MeV protons in silicon [27]. (b) Schematic of the damage profile and deflected hole current around high defect region during anodization. (c) Schematic of electrochemical anodization process in which the end-of-range region remains as solid silicon. (d) Basic shapes that can be machined on PSi and silicon surfaces.