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Crosstalk-aware multi-bit flip-flop generation for power optimization ☆, ☆☆

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ABSTRACT

Applying multi-bit flip-flops (MBFFs) for clock power reduction in modern nanometer ICs has been becoming a promising lower-power design technique. Many previous works tried to utilize as more MBFFs with larger number of bits as possible to gain more clock power saving. However, an MBFF with larger number of bits may lead to serious crosstalk due to the close interconnecting wires belonging to different signal nets which are connected to the same MBFF. This paper analyzes, evaluates, and compares the relationship between power consumption and crosstalk when applying MBFFs with different numbers of bits. To solve the addressed problem, a novel crosstalk-aware power optimization approach is further proposed to optimize power consumption while satisfying the crosstalk constraint. Experimental results show that the proposed approach is very effective in crosstalk avoidance when applying MBFFs for power optimization.

1. Introduction

Power/thermal minimization has been becoming one of the most important objectives in the design of modern system on chips (SOCs) which integrate huge numbers of transistors. High power/thermal dissipation of an SOC may degrade product lifetime and reliability. The power consumption of an SOC arises from dynamic, leakage, and short-circuit power, where the dynamic power is the major power source among the three [2]. The power consumption of the clock network further dominates the dynamic power [3] because of the highest switching rate of the clock signal.

To minimize the power consumption of the clock network, many techniques had been proposed, such as buffer sizing [4,5], clock gating [6,7], register clustering [8,9] and banking [10], and replacing 1-bit flip-flops with multi-bit flip-flops (MBFFs) [11–19]. Recent studies have shown the effectiveness of applying MBFFs in saving both power and area [11–13,16,18,19].

An MBFF consists of two or more 1-bit flip-flops, which share a common clock driver as shown in Fig. 1. The clock driver usually consists of two inverters that generate opposite phase clock signals for master and slave latches. According to [16], as the process technology advances to 65 nm and beyond, the minimum-sized clock driver can still drive several flip-flops. Consequently, replacing 1-bit flip-flops with MBFFs can reduce the power consumption of the clock network and the chip area due to the elimination of redundant clock drivers.

In addition to the reduction of flip-flop power consumption and chip area, some previous works [15,16] also presented other advantages of applying MBFFs. For example, common clock and enable signals for a group of flip-flops and reduced depth of a clock tree make clock skew more controllable. With fewer clock sinks and smaller capacitive load on the clock net, the delay and power consumption of the clock network can be improved. When considering design for testability (DFT) with MBFFs, the required routing resource utilization for a scan chain will be greatly reduced.

1.1. Previous work

The idea of applying MBFFs was first proposed in [15] to control clock skew and delay during physical synthesis. Kretchmer [14] and Chen et al. [16] introduced a design methodology to infer MBFF cells using existing logic synthesis tools. Based on the MBFF inference, it is possible to map an RTL design directly to a gate-level design with MBFF cells.

Recent studies suggested to apply MBFFs at the placement stage for better timing budgeting. All of the previous works

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[11–13,17–21] formulated the problem of replacing 1-bit flip-flops with MBFFs by minimizing flip-flop power consumption or the number of clock sinks while satisfying both timing and placement density constraints. Some of them additionally considered wirelength minimization [11–13,17], routability [18,19], and clock latency [20]. However, applying MBFF may also introduce substantial crosstalk noise among the signal nets. Fig. 2 illustrates examples of merging eight 1-bit flip-flops into one 8-bit flip-flops may result in serious crosstalk when an newly generated MBFF connects to the pins which are closed to each other. According to [22], serious crosstalk noise will result in unnecessary glitch and increase transition time on signal nets leading to functional failure. Fig. 3 gives two examples of signal anomalies. In Fig. 3(a), if one of the wires is switching, while the other one is stable, there will be a glitch on the stable wire. In Fig. 3(b), if two wires are simultaneously switching in opposite phases, the transition delay will be increased. Therefore, it is required to minimize crosstalk noise when applying MBFFs for power reduction.

1.2. Our contributions

In this paper, we address the crosstalk effect when applying MBFFs for clock power saving. We observe the ineffectiveness of applying MBFFs with larger number of bits due to serious crosstalk based on the crosstalk evaluation. We also propose a new problem formulation, which additionally consider the crosstalk constraint when applying MBFFs for clock power saving. Unlike the existing power optimization flows with MBFFs without considering crosstalk effect or merely considering routability during MBFF placement, we introduce the coupling capacitance map and present a novel algorithm to avoid crosstalk effect during Flip-Flop merging and MBFF placement. The key contributions are summarized in the following:

- We evaluate, analyze, and compare the relationship between power consumption and crosstalk when applying MBFFs with different numbers of bits, and address the ineffectiveness of applying MBFFs with larger number of bits due to the serious crosstalk.
- To solve the addressed problem, a novel crosstalk-aware power optimization flow and the corresponding algorithms are proposed to minimize power consumption while satisfying the crosstalk, timing, and placement density constraints.
- We present a crosstalk-aware bottom-up clustering algorithm for better crosstalk consideration instead of clustering a maximum number of 1-bit flip-flops by searching the maximum clique in the flip-flop intersection graph [11–13,17]. A coupling capacitance map is also introduced for better crosstalk estimation throughout the algorithms.
- Compared with our preliminary version [1], we improve the objective for flip-flop clustering, and introduce the new crosstalk-aware MBFF placement algorithm for better considering crosstalk.
- Experimental results show that the proposed approach is very effective in crosstalk avoidance when applying MBFFs for power optimization compared with the previous works.

The remainder of this paper is organized as follows. Section 2 demonstrates the crosstalk effect due to MBFFs. Section 3 presents a new problem formulation for placement-based power optimization with MBFFs to mitigate the crosstalk effect. Section 4 proposes our algorithms to solve the problem. Section 5 reports the experimental results, and finally Section 6 concludes this paper.

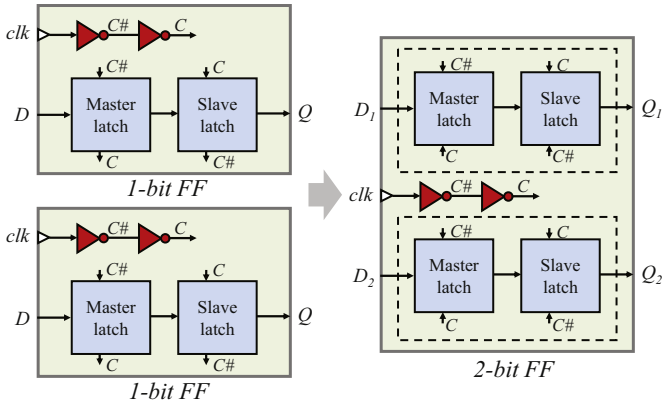

Fig. 1. An example of merging two 1-bit flip-flops into one 2-bit flip-flop [11,12].

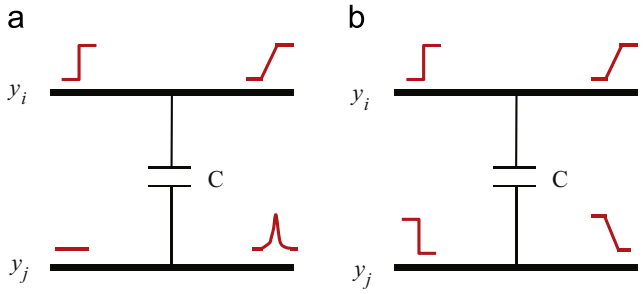

Fig. 3. Two examples of signal anomalies [22]. (a) Glitch. (b) Delay.

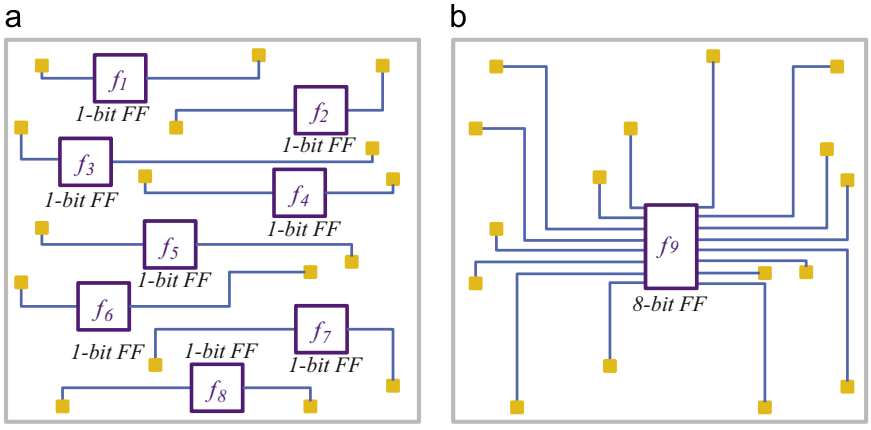

Fig. 2. An example of merging eight 1-bit flip-flops into one 8-bit flip-flop resulting in serious crosstalk among the connected signal nets.