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SIAR: Customized real-time interactive router for analog circuits ☆

Hailong Yao [a,*], Fan Yang [a], Yici Cai [a], Qiang Zhou [a], Chiu-Wing Sham [b]

[a] Department of Computer Science and Technology, Tsinghua University, China
[b] The Hong Kong Polytechnic University, Hong Kong

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ABSTRACT

As analog and mixed-signal (AMS) circuitry gains increasing portions in modern SoCs, automatic analog routing is becoming more and more important. However, routing for analog circuits has always been an extremely challenging task due to complicated electrical and geometrical constraints. Due to these constraints, current analog routers often fail to obtain a routing solution that the designer wants. To incorporate the designer's expertise during routing, a customized real-time interactive analog router is attracting increasing concerns in industry.

This paper presents a fast customized real-time interactive analog router called SIAR. A key feature of SIAR is that it allows for real-time interactions between the router and the designer. The designer can try different *guiding points* by moving the cursor in the user window and SIAR will return and display the corresponding routing solution in real-time, such that the designer could choose the most satisfactory one. The guiding points are very important for the designer to obtain satisfactory routing solutions, even for routing solutions with analog matching constraints by setting symmetric guiding points. A new splitting graph based routing model is presented to efficiently search the routing path and record the number of turns/vias during searching by efficient tile splitting operations. SIAR supports different routing modes such as point-to-point, point-to-module and module-to-module. An efficient connecting point selection method is presented such that an optimal routing solution is preserved when connecting to a module. Different design rules such as variable wire and via width/spacing rules, along with the same-net spacing rules, are supported in SIAR. Moreover, a global routing stage is presented to speedup the routing process for large designs. Experimental results are promising.

1. Introduction

With the continuous advancement of IC manufacturing process, it is possible to fabricate analog and mixed-signal (AMS) circuits at 45 nm technology nodes and below [1], which boosts the AMS development and increases the portions of AMS parts in modern SoCs. This brings new challenges to analog design automation especially for analog routing. Routing for analog circuits has been a completely manual, time-consuming and error-prone task [2], which typically needs many iterations and becomes the bottleneck in the whole analog design flow. Automatic analog routing will greatly improve the designer's productivity and reduce the design cycle time. However, due to the complexity of the stringent analog routing constraints and the pursuit of high circuit performance, pure automatic router does not perform so well for sensitive analog nets as it is for digital signal nets. That is, automatic analog router is not intelligent enough to handle all kinds of routing constraints and requirements properly. In most cases, the designer wants to guide the path searching process, especially for those sensitive analog nets, such as nets with electrical and/or geometrical matching constraints. Therefore, a customized real-time interactive analog router is attracting more and more concerns in industry, which enjoys both the routing efficiency and the merit of including designers' expertise.

There have been some research works on analog design automation. In [3], the constraint-driven physical design is discussed. In [4], an area routing method is presented for analog circuits with performance cost and shielding using the tile-based routing model, which may suffer from low routing efficiency. Besides, it does not consider the design rules of vias, etc. In [5,6], analog placement and routing approaches are presented with symmetry constraints. In [7], a matching-based placement and routing system is presented using matching patterns. In [8,9], the current-driven routing methods are presented based on Steiner tree and terminal tree, respectively. In [10], an analog shielding

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* Corresponding author. Tel.: +86 10 62795403; fax: +86 10 62781489.
E-mail addresses: hailongyao@tsinghua.edu.cn (H. Yao), fyang06@gmail.com (F. Yang), caiyc@tsinghua.edu.cn (Y. Cai), zhouqiang@tsinghua.edu.cn (Q. Zhou), encwsham@polyu.edu.hk (C.-W. Sham).

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routing algorithm is presented by net classification to handle different performance requirements of different nets. Due to the importance of constraints in analog circuits, more and more designs start to adopt the constraint-driven methodology [3,11,12,13,14]. However, few research works in literature are on the analog routing methods with real-time and interactive applications [19,20].

Most automatic analog routers adopt the gridless routing model because of its capability of dealing with variable line width and spacing rules. Generally, the gridless routing model can be categorized as implicit-connection-graph-based and tile-based according to different representations of the routing region. In [15], a connection graph is constructed by expanding all the obstacles and then extending the boundary lines of the obstacles. The boundaries may become too dense with the increase in the number of obstacles, which will greatly slow down the path searching process. In [16–18], the routing region is partitioned into rectangular shapes called "tiles", where a tile can be either a space tile or a block tile. However, the total number of vias/turns within the tiles cannot be estimated accurately during the path searching process, thus resulting in a routing solution with unnecessary vias/turns. As is known that vias/turns should be reduced because they degrade the circuit performance and reliability. Therefore, the above two classes of routing methods either suffer from the runtime issue or generate degraded routing solutions.

An interactive router can be regarded as a semi-automatic router which allows the designer to guide the path searching process using *guiding points*. A guiding point can be input by a cursor as the designer moves or clicks the mouse in the user window. The designer typically wants to try different guiding points to find the most satisfactory routing path. A guiding point is very important to the designer especially for sensitive net with electrical and/or geometrical matching constraints. An efficient router that can respond in real-time is necessary in this context. Moreover, the designer may want to specify customized requirements for different nets before routing. These requirements include available routing layers, routing costs (e.g., unit cost for horizontal/vertical wires, cost for turns on each layer, cost for vias, etc.), and routing constraints such as line width, spacing, and the size of via arrays. This paper presents such a customized real-time interactive router called SIAR based on a new splitting graph. In SIAR, the routing efficiency is greatly improved based on the new splitting graph such that the designer can freely move the cursor and the computed optimal routing paths corresponding to the cursor positions are shown in real-time. SIAR greatly saves the designer from manual path connection tasks which is error-prone due to complicated design rules.

In analog circuits, the pins of analog nets are typically rectilinear polygonal shapes (in this paper we call them *modules*). A path searching procedure from one module to another is called *module-to-module routing*. It is difficult to guarantee optimal routing solutions using the gridless routing model. The number of possible connection points of a module is theoretically infinite in gridless routing and the selected subset of connection points determine whether the optimal solution is preserved in the reduced solution space. This paper presents a method to choose a subset of connection points on a module such that at least one of the optimal routing paths to the module is available. That is, the solution space corresponding to the chosen subset of connection points contains at least one optimal routing solution.

Moreover, SIAR considers more practical routing constraints. Typical design rules such as minimum line width, minimum line spacing, and rules for vias are all supported. Besides, the same-net spacing rule is also supported, which is one of the most important constraints for analog circuits. The same-net spacing rule is the constraint for the minimum spacing between the net being routed and other same-net pre-routes. These pre-routes of the same net are considered as obstacles, though they are electrically equivalent to the current routing path. For example, when the user sequentially input several guiding points during routing, the accepted routing paths between previous guiding points are considered as the same-net pre-routes. These same-net pre-routes are considered as obstacles, and the same-net spacing rule should be guaranteed. SIAR deals with the same-net spacing constraint in the splitting graph construction procedure and guarantees the routing solution without design rule violations.

In SIAR router, a new splitting-graph-based routing approach is presented, which guarantees to find an optimal routing solution considering the wirelength and the number of vias and/or turns, with enhanced routing efficiency. The main contributions are as follows:

- A new splitting graph is proposed to represent the routing region. During the path searching process, the tiles in the graph are efficiently split to record the number of vias/turns. Thus, an optimal routing solution is guaranteed with minimized vias/turns.
- Module-to-point and module-to-module routing methods are proposed with an effective connection point selection method on the module boundaries. The connection point selection method ensures that an optimal routing solution exists.
- Effective methods are presented in SIAR to successfully handle different analog routing constraints including the same-net spacing constraint.
- A global routing stage with new gcell cost metrics is integrated to speedup SIAR router for large designs.

The rest of this paper is organized as follows. Section 2 gives an overview of SIAR router. Section 3 presents details of the splitting graph. Section 4 discusses the module-to-module routing. Section 5 covers the same-net spacing constraint. Section 6 presents the detailed searching process on the splitting graph. Section 7 presents the global routing stage for routing speedup. Section 8 gives the whole flow. Section 9 presents the experimental results. Section 10 concludes the paper with further research directions.

2. Overview of SIAR

2.1. Problem formulation

For SIAR router, the input consists of the following parts: (1) user-specified routing source and target, which can be either modules or guiding points, (2) the routing layout data based on OA database [23], (3) the technology library with the default design rule constraints including minimum line width, minimum line spacing, via related design rules, the same-net spacing design rules, etc., and (4) customized input from User Interface including available routing layers, available vias with user-specified via enclosure values, customized line width and line spacing, and unit-length routing cost for horizontal and vertical routing directions on each routing layer. When the user specification is not valid, e.g., when the user-specified line width is less than the minimum design rule of the technology library, the values from the technology library are used.

When all the input data are loaded and processed, the routing problem can be stated as follows:

Input: (1) a set of rectilinear polygons and rectangles as the routing obstacles, (2) modules or points as the routing source and routing target, and (3) available routing layers and vias, along with