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# Floorplan-aware analog IC sizing and optimization based on topological constraints ☆

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ABSTRACT

This paper presents a methodology for analog IC circuit-level sizing and optimization, which takes into account the layout geometrical properties, by introducing a simple and general description that permits the inclusion of the floorplan generation in the sizing optimization loop with negligible computational costs. The usage of a modified NSGA-II state-of-the-art multi-objective multi-constraint optimization kernel enables the efficient exploration of design tradeoffs, while the inclusion of corner cases and the usage of the industrial circuit simulators (HSPICE®, Eldo® or Spectre®) ensures the accuracy and reliability of the solutions. Several layout templates that enclose the constraints defined by the designer are used to generate multiple floorplan solutions for each sizing solution during the synthesis process, giving the optimizer pertinent and accurate geometric layout information, e.g., area, width, length, wasted area, etc. Additionally, a built-in technology independent module generator facilitates the instantiation of multiple versions of each device, further increasing the exploration of possible geometric combinations and consequently packing of the floorplan with a minimum of wasted area. The developed tool, AIDA-C, implements the proposed approach, and is validated for both classical and new analog circuit structures using the UMC 130 nm design process.



## 1. Introduction

Although most functions in today's integrated circuits (ICs) are implemented using digital signal processing circuitry, analog circuits still play a major role. Analog blocks acquire and produce the continuous-valued signals that exist in the world, leading to complex systems-on-a-chip (SoC) where digital and analog circuits are integrated together on the same die [1]. Unlike digital circuits, where the low-level phases of the design process are automated using fairly standard methodologies, the synthesis and layout of analog circuits is either a manual task or uses some kind of custom automation solutions. The lack of effective computer-aided-design (CAD) tools for electronic design automation (EDA) in the analog domain is one of the main reasons for the large development cycle of the analog blocks [2]. The absence of mature design automation tools creates a great dependence on human intervention in all phases of the design process, which, despite being supported by circuit simulators, layout editing environment and verification tools, result in a time-consuming and error-prone design flow.

One of the major tasks in the design flow of analog ICs is circuit sizing. The automation of analog circuit sizing is commonly achieved using optimization-based techniques that may or may not use a circuit simulator to evaluate the performance of the tentative solutions during the synthesis process [1]. Some commercially available solutions, like the circuit optimizer feature of Cadence's Virtuoso Custom Design Platform GXL [3], Synopsys Titan ADX [4] or MunEDA-GNO [5] already implement such an optimization-based approach. However, in these tools limitative single-objective approaches are taken, where a single performance value to provide only one solution, not showing the tradeoff landscape to the designer, furthermore, no layout-related data is included within these frameworks.

Traditionally, the next task of the design flow is the layout synthesis, in this phase the fabrication masks that are used to produce the devices are drawn using the sizes obtained from the previous step. To overcome the increasing impact of layout parasitic effects in circuit's performance, sizing and layout design phases tend to overlap. Integrating layout generation or

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layout-related data in the sizing optimization process helps trim down the effects of high-order non-idealities and parasitic disturbances that affect analog circuits' performance [6]. However, both complete layout generation and parasitic extraction are still time consuming tasks. This time cost appears either in the processing time, when using custom automatic layout generator plus layout extraction inside the sizing optimization loop [7], or in the design time of circuit specific procedural generators, that code the entire layout of a circuit in a tool, with parasitic estimation [6,8,9]. Fig. 1 illustrates the different evaluation techniques that are used in optimization-based circuit synthesis.

This paper presents a methodology for general purpose automatic simulation-based sizing and optimization of analog IC that takes into consideration layout geometrical constraints. Unlike previous layout-aware works, where the complete layout is generated and extracted using post-extracted performance values during the optimization [6,7], in this work a set of floorplan constraints providing a general, simple-to-derive, fast-to-compute and accurate geometric layout estimate to be used during the circuit optimization. In our approach, instead of the time-consuming complete layout generation and extraction to control the parasitic effects, the undesirable layout induced effects are alleviated by using the designer experience to define using simple constructs where and how to lay out the devices. By enforcing matching, symmetry and proximity constraints on the individual devices, and by further increasing matching using complex layout structures like common-centroid or interdigitated [10], the deviations due the fabrications process, as observed in [11], are reduced thus shortening the gap between pre- and post-layout circuit simulation [12]. The new circuit optimizer, AIDA-C, which evolved from GENOM-POF [13] in the AIDA framework [14], implements the proposed floorplan-aware automatic synthesis flow and is used to demonstrate its effectiveness. To further increase the geometric exploration during synthesis, while generating the complex layout structures, a new Analog Module Generator (AMG) that extends the degrees of freedom explored during the synthesis, delivering a wide range of layout alternatives for each device, is used. The AMG is a component of AIDA framework and is integrated with both, AIDA-C and AIDA-L. AIDA-L is AIDA's automatic layout generator tool that resulted from the maturation and integration of the LAYGEN-II [15,16] in the framework.

This paper is organized as follows. In Section 2, an overview of the related work in automatic analog IC circuit-level synthesis is presented. Section 3 introduces the AIDA framework, and in Section 4 the complete floorplan-aware circuit synthesis, implemented in AIDA-C, is described. Then, in Section 5 the methodology is illustrated with two case studies, and finally, in Section 6, the conclusions are drawn.

## 2. Related work

Optimization-based synthesis is the most common approach to automatic circuit synthesis at circuit level, and some flavors of it are already integrated and available in the toolkits provided by most EDA providers. These approaches are preferred to design plans [17,18], because they provide hard to derive, require constant maintenance and yield non-optimal solutions. Optimization-based approaches are not without their shortcomings, especially the long time required to evaluate the circuit performance when accurate circuit simulators are used [6,13,19,20,21]. Nevertheless, given the computational capabilities available in today's workstations the discovery of quasi-optimal solutions is achieved within acceptable time frames. Moreover, the electrical circuit simulator is probably the most well established tool in the analog design flow, being used to verify the performance of the circuit since early design stages until the post-layout validations. Using the circuit simulator eases the inclusion of automation in the design flow, while maintaining confidence in the obtained solution. Moreover, unlike equation-based approaches, such as [21], that require circuit specific equations, the scope of the circuit simulator is general. In order to increase the performance of simulator-based circuit optimizers, surrogate-based evaluation is maturing as an alternative technique to avoid the costly simulations [22]. In such approaches, the global accuracy of the simulator is traded by the speed of applying the surrogate model for performance estimation. These models are automatically generated which eases design and maintenance, however tuning the model accuracy can be complicated, which makes them hard to use in a generalized form.

Furthermore, to achieve post-layout successful designs that meet all specifications requires time-consuming and non-systematic iterations between electrical and physical design phases. Moreover, as layout induced parasitic effects strongly affect the performance of analog circuits, even the evaluation of the circuit area or aspect ratio is practically impossible from the netlist alone. Thus, to address post-layout performance degradation earlier in the design flow, the, so called, layout-aware or layout-driven design approaches include layout effects during the sizing loop, therefore, ensuring post-layout performance of the attained solutions.

Without actually generating the layout, in [8] device parasitic effects are modeled by linear regression from a Pareto optimal surface, obtained by sampling the design space and using a procedural layout generator to produce the layout for each point, where such solution is aware of its specific layout induced effect. In [9] the layout is produced by a parameterized layout generator,

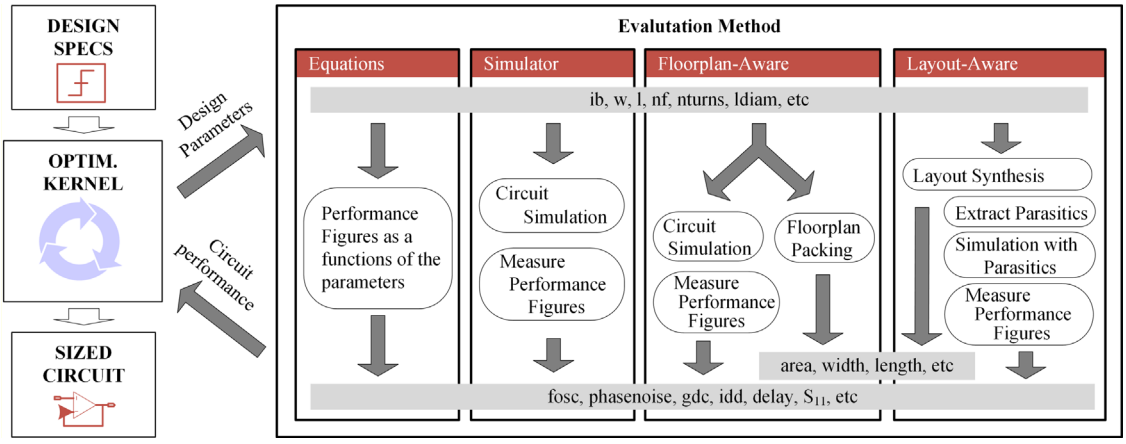


**Fig. 1.** Alternative evaluation methods for optimization-based synthesis of analog IC.