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Fast multidimensional optimization of analog circuits initiated by monodimensional global Peano explorations

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ABSTRACT

A fast design space exploration of analog firm intellectual properties (IP) based on Peano-like paths (piecewise linear and monodimensional) is presented. First, the *n*-dimensional design space is globally explored following those Peano curves, which are obtained by varying only 1 design variable at a time using a fixed step size. Each variable is taken within a given range. During exploration, the best *x-percentile* points are retained. After varying globally the *n* variables, a Nelder–Mead simplex optimization is performed using each of the best points as an initial point. Successive *p*-variable partitioning of the *n*-dimensional design space (with $p \ll n$) are applied to adapt the simplex optimization to large dimensions. The proposed exploration technique is combined with a simulation-based hierarchical sizing and biasing methodology to size and bias analog firm IPs. This combined approach has been successfully applied to size and bias a Constant Voltage Reference (*CVR*) in a 5 V SOI 1 µm technology. The results illustrate the effectiveness and accuracy of the proposed approach.

1. Introduction

Over the past few decades, research in analog synthesis led to the emergence of 2 major schools: the first school pushing towards *Full Design Automation* (*FDA*) and the second school pushing towards *Full Design Handcrafting* (*FDH*). Many academic and commercial tools have been introduced by the FDA school such as OASYS [1], DELIGHT.SPICE [2], ASTRX/OBLX [3], AMGIE [4], ANACONDA [5], MOBU [6], WiCkEd [7], NEOLINEAR ACQUIRED by Cadence and Analog Design Automation Inc. acquired by SYNOPSYS. Except for OASYS and AMGIE which are knowledge-based, the tools were mainly simulation-based for its generality. On the other hand, few academic tools have been introduced by FDH school such as COMDIAC [8], PAD [9,10] and [11,12], which provide analog designers with sufficient insight for full trade-offs optimization.

Over many years, analog designers built sufficient expertise to analyze real complex circuits. However, for such complex circuits, FDA tools require important preparatory effort, have large execution times and the final design is not always optimal. Today, analog designers seek to develop structured design methodologies that provide: *physics-based design*, *capacity to deal with complex circuits*, *bridging the gap between hand analysis and simulation*, *sufficient design insights*, *performance trade-offs exploration* and *analog design assistance*.

In an attempt to meet the above requirements, we presented in [13] a methodology for hierarchical sizing and biasing of analog firm IPs. The previously proposed methodology elaborates an intermediate design representation, called *dependency graphs*. These were used to represent sizing procedures and ensure their consistency, reusability and technology independence. By construction the procedure fulfilled topology constraints, designer's hypotheses and design constraints. These procedures were evaluated to size and bias transistors of the corresponding analog firm IP. The procedures could be stored in an XML database for later use. Potential contributions to the field of synthesis and simulation were illustrated. For synthesis, the concept of *knowledge-aware synthesis* was presented. We showed that introducing dependency graphs inside optimization loops accelerates the optimization process and highly reduces the design space for the same analog IP.

In knowledge-aware synthesis, it is assumed that performance equations are provided by the designer for the underlying topology. These are expressed using circuit parameters resulting from the evaluation of dependency graph.

As a first contribution in this paper, we extend the concept of knowledge-aware synthesis by replacing the performance equations by traditional SPICE-like netlists that are much easier to provide. As a second contribution, we will introduce a novel optimization algorithm that is more efficient to use with the

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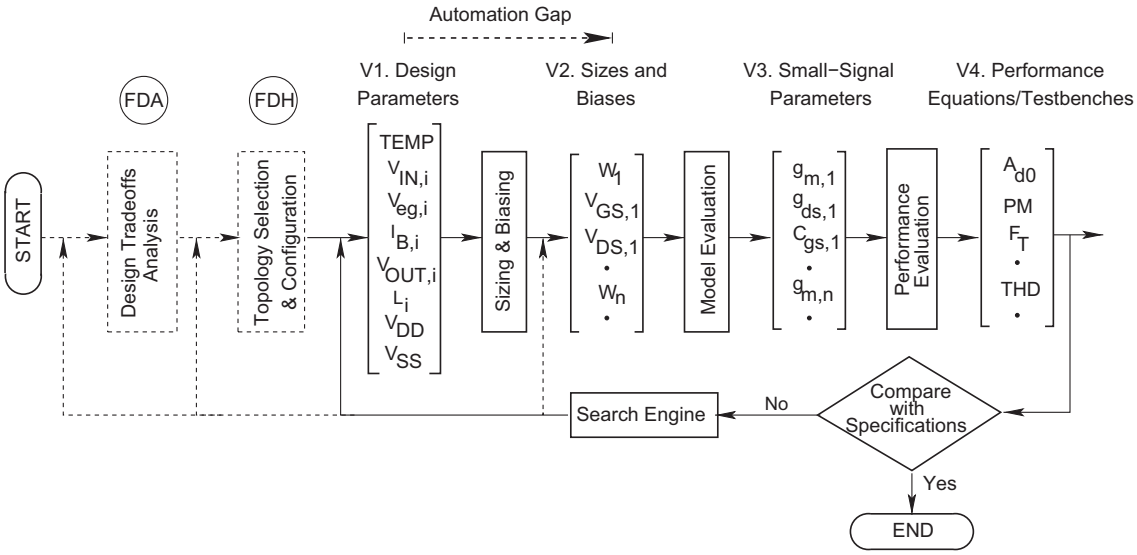

Fig. 1. Proposed loop for circuits optimization.

hierarchical sizing and biasing methodology [13]. The overall resulting simulation-based methodology is shown to be efficient in optimizing complex analog firm IPs.

The paper is organized as follows. Section 2 defines the problem. Section 3 gives an overview of the hierarchical sizing and biasing methodology. The proposed optimization engine is introduced in Section 4. Section 5 presents the test functions and impact of optimizer parameters. The optimization and simulation results of a CVR circuit are reported in Section 6. Finally, Section 7 concludes the paper.

2. Problem definition

To further analyze the challenges in analog design automation, the tasks involved in both knowledge-based and simulation-based syntheses are presented in Fig. 1.

Simulation-based synthesis encapsulates a simulator within an optimization loop. Since the simulator is a verification tool, it starts with a set of sizes and biases (vector V2). First, it computes small-signal parameters (vector V3) by evaluating transistor models such as BSIM3V3, BSIM4, PSP and EKV. Second, linear and nonlinear performances (vector V4) are evaluated using a set of test benches. We point that *model evaluation* and *performance evaluation* are performed by the simulator. The search engine uses sizes and biases (vector V2) as optimization variables. It leaves both *model evaluation* and *performance evaluation* to the simulator. This approach is illustrated by the innermost loop of Fig. 1. In operating-point-driven formulation [4], the optimizer optimizes the circuit design parameters (vector V1) as in the solid-line loop of Fig. 1. In this case, complex sizing and biasing procedures are manually written to ease the mapping from vector V1 to vector V2 [1,3,4].

On the other side, knowledge-based synthesis is very cumbersome. Using the circuit design parameters (vector V1), the designer codes complex sizing and biasing procedures to compute sizes and biases (vector V2). From vector V2, the designer uses simplified transistor models for model evaluation. Finally, the designer extracts approximate equations for performance evaluation.

Since the designer wishes to use more intuitive design parameters (vector V1), and that simulation-based synthesis tools starts from sizes and biases (vector V2), we identify an *automation gap* in the analog design flow illustrated in Fig. 1.

In [13], our main contribution was to automate the mapping from circuit design parameters (vector V1) to sizes and biases (vector V2). Meanwhile, standard transistor models were used. In the sizing and biasing phase, sizing procedures were automatically generated based on topology constraints, designer's hypotheses and design constraints. This was achieved by proposing a new intermediate representation called *dependency graphs* to express knowledge and ensure its consistency, reusability and independence on technology.

One major point was the performance evaluation. In general, performances are classified into 3 categories: *linear*, *weakly nonlinear* and *strongly nonlinear*. Linear and weakly nonlinear performances may be easily modeled using mature symbolic analysis techniques [14,15]. Strongly nonlinear performances may be modeled using various techniques such as *model-order reduction* [16], *support vector machines* [17] and many others. Due to the complexity in integrating these techniques in our previously proposed method [13], we assumed that performance equations were mainly provided by the designer.

Since the development of performance equations especially in the strongly nonlinear case is very laborious, we propose the simulation-based version of the hierarchical sizing and biasing methodology where performances in vector V4 of Fig. 1 are evaluated using test benches that are easier to manipulate by the designer. The use of test benches for performance evaluation are easily applied for linear and nonlinear performances since SPICE-like simulators provide directly these types of analyses.

3. Hierarchical sizing and biasing methodology

The hierarchical sizing and biasing methodology [13] generates suitable sizing procedures that respect the designer's choice of input parameters and constraints. A sizing procedure is a sequence of sizing and biasing operators that are described in the next subsections. The hierarchical sizing and biasing methodology is implemented as part of the platform CHAMS.

3.1. Main idea

Assume that the width of a MOS transistor is to be computed at ambient temperature. The MOS transistor model is given by

$$I_{DS} = F_{1,model}(Temp, W, L, V_{GS}, V_{BS}, V_{DS}) \quad (1)$$